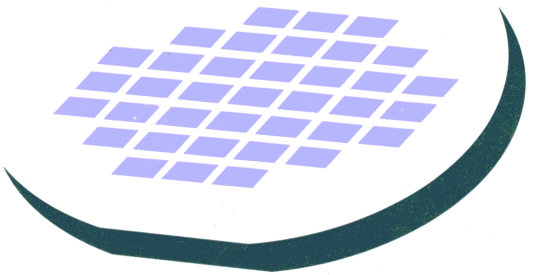

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DATA BOOK
1991

STARTECH
PRODUCT DATA BOOK 1991

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PRODUCT LIST

ST16C450	Low power CMOS universal serial transmitter and receiver.
ST16C2450	Low power CMOS Dual universal serial transmitter and receiver.
ST16C454	Low power CMOS Quad universal serial transmitter and receiver.
ST16C452	Low power CMOS Dual universal serial transmitter and receiver with parallel printer port.
ST16C550	Low power CMOS universal serial transmitter and receiver with 16 byte FIFO.
ST16C2550	Low power CMOS Dual universal serial transmitter and receiver with 16 byte FIFO.
ST16C554	Low power CMOS Quad universal serial transmitter and receiver with 16 byte FIFO.
ST68C554	Low power CMOS Quad universal serial transmitter and receiver with 16 byte FIFO for Motorola , Rockwell, Hitachi and similar base microprocessors.
ST16C552	Low power CMOS Dual universal serial transmitter and receiver with 16 byte FIFO and parallel bidirectional printer port.
ST84C71	Low power CMOS 16 bit IDE interface with floppy and hard disk decode logic.
ST26C31	Low power CMOS high speed Quad RS-422, RS-423 differential line driver.
ST34C87	Low power CMOS high speed Quad RS-422, RS-423 differential line driver.
ST26C32	Low power CMOS high speed Quad RS-422, RS-423 differential line receiver.
ST34C86	Low power CMOS high speed Quad RS-422, RS-423 differential line receiver.
ST86C87	Low power CMOS high speed Dual RS-422, RS423 differential line receiver and driver.
ST41C76	Low power CMOS high speed 6 bit video DAC.

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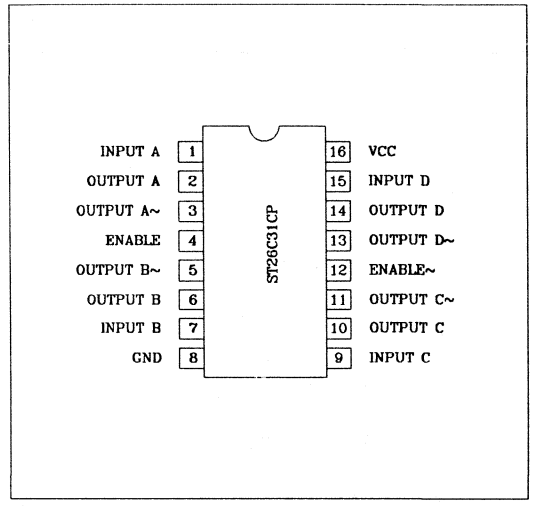
COMMUNICATION

1

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST26C31 is a CMOS quad differential line driver,designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signal special hysteresis is built in the ST26C31 circuit.



FEATURES

* Pin-to-pin compatible with National DS26C31C
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

APPLICATIONS

* Hard disk drives
* RS-422 controller cards
* MFM / RLL controller cards
* Digital line transmission driver

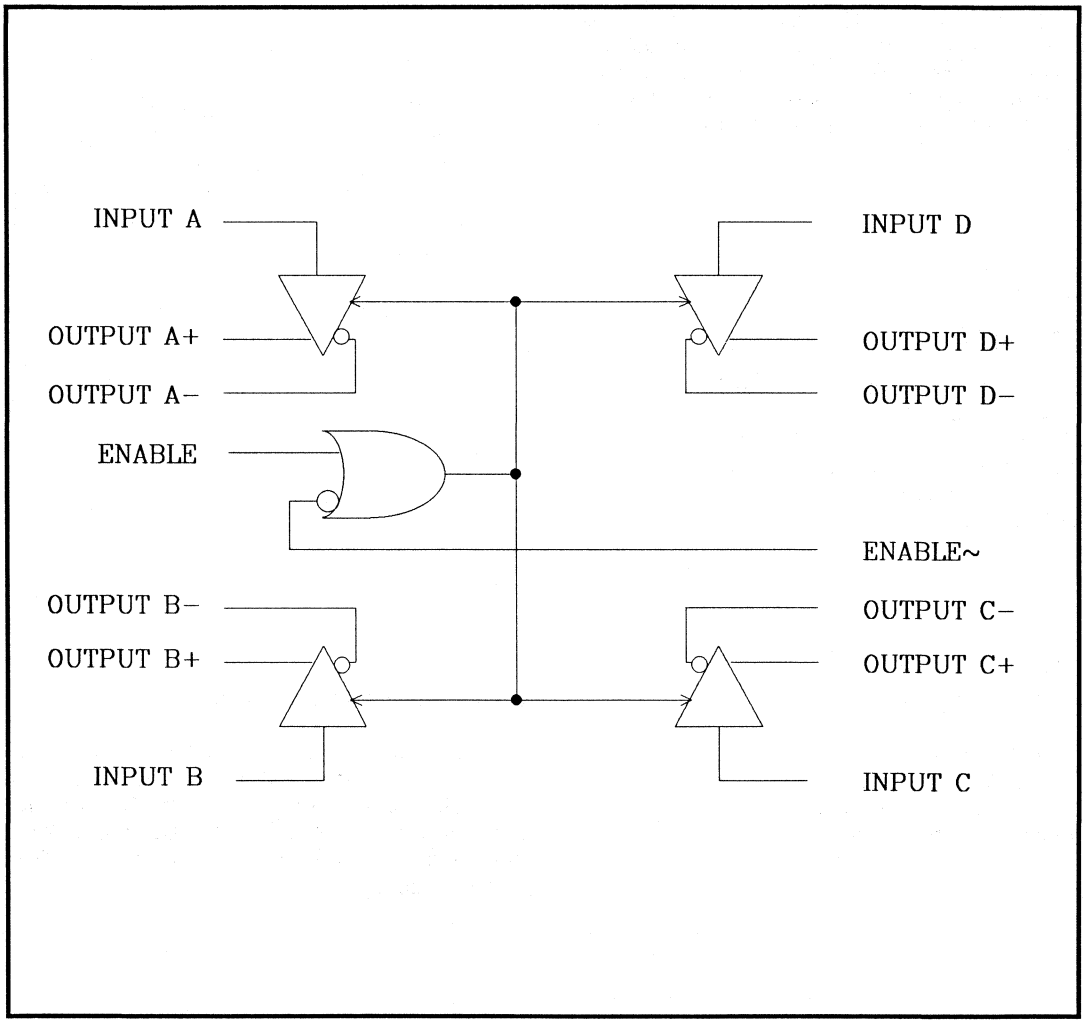
GENERAL DESCRIPTION

The ST26C31 is a high speed CMOS line driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C31CP16	Plastic	0° C to + 70° C
ST26C31CJ18	PLCC	0° C to + 70° C

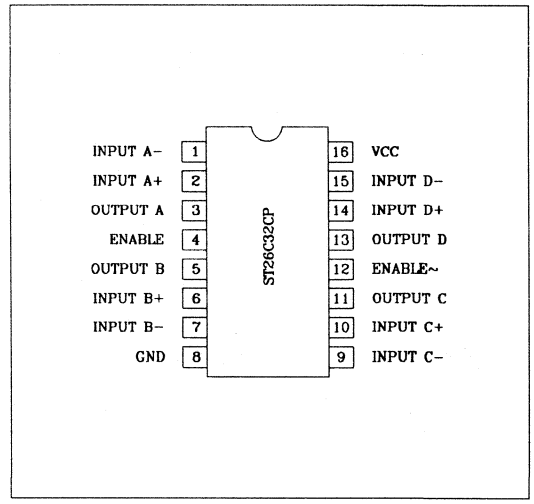
BLOCK DIAGRAM



QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver,designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of +/- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.



FEATURES

* Pin-to-pin compatible with National DS26C32C
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

APPLICATIONS

* Hard disk drives
* RS-422 controller cards
* MFM / RLL controller cards
* Differential transmission receiver

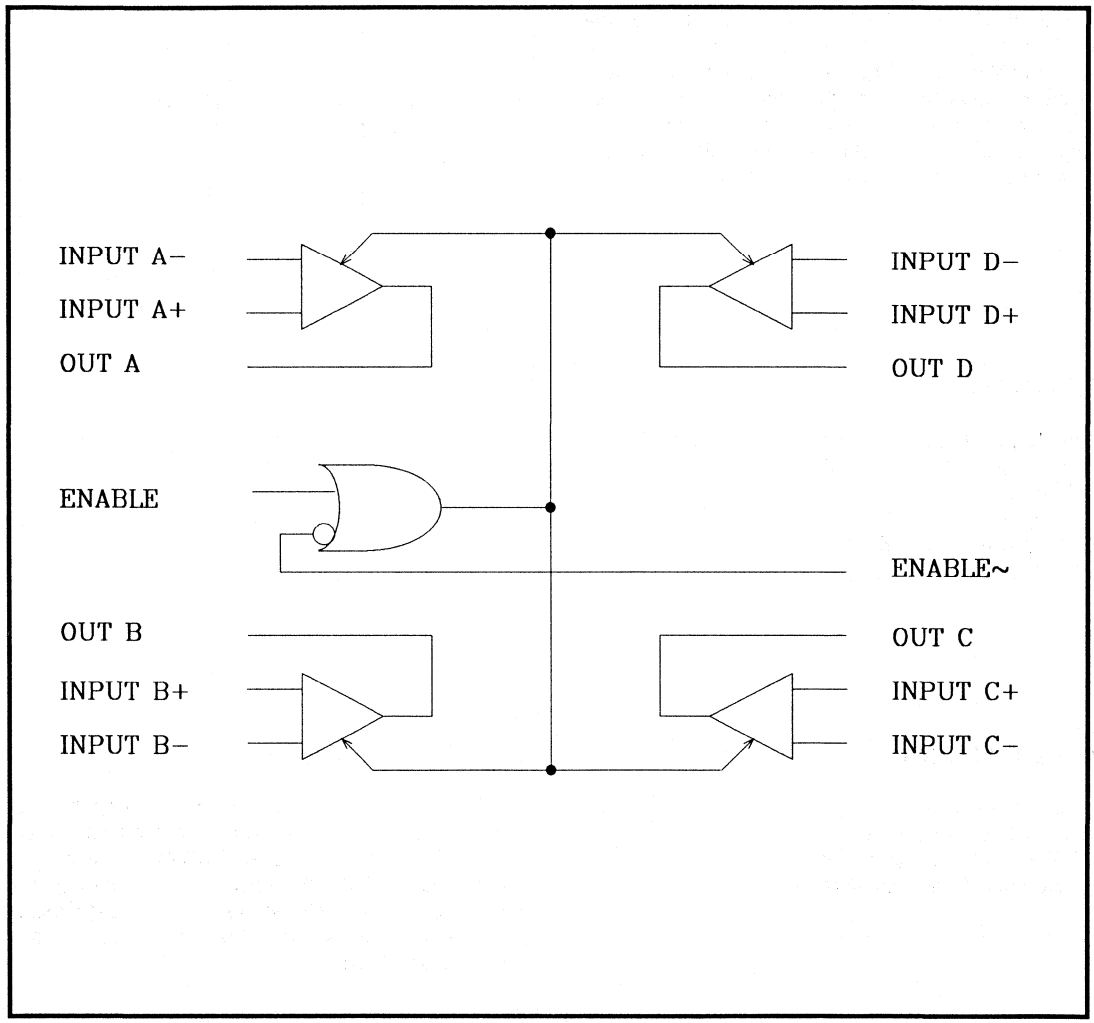
GENERAL DESCRIPTION

The ST26C32 is a high speed line receiver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic	0° C to + 70° C
ST26C32CJ18	PLCC	0° C to + 70° C

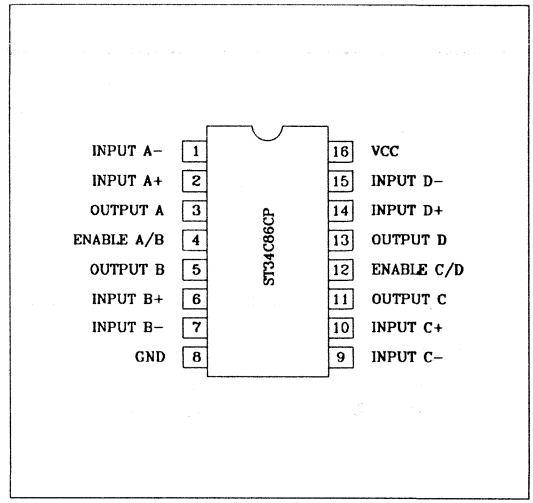
BLOCK DIAGRAM



QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver,designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of + /- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.



FEATURES

* Pin-to-pin compatible with National DS34C86
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

APPLICATIONS

* Hard disk drives
* RS-422 controller cards
* MFM / RLL controller cards
* Differential transmission receiver

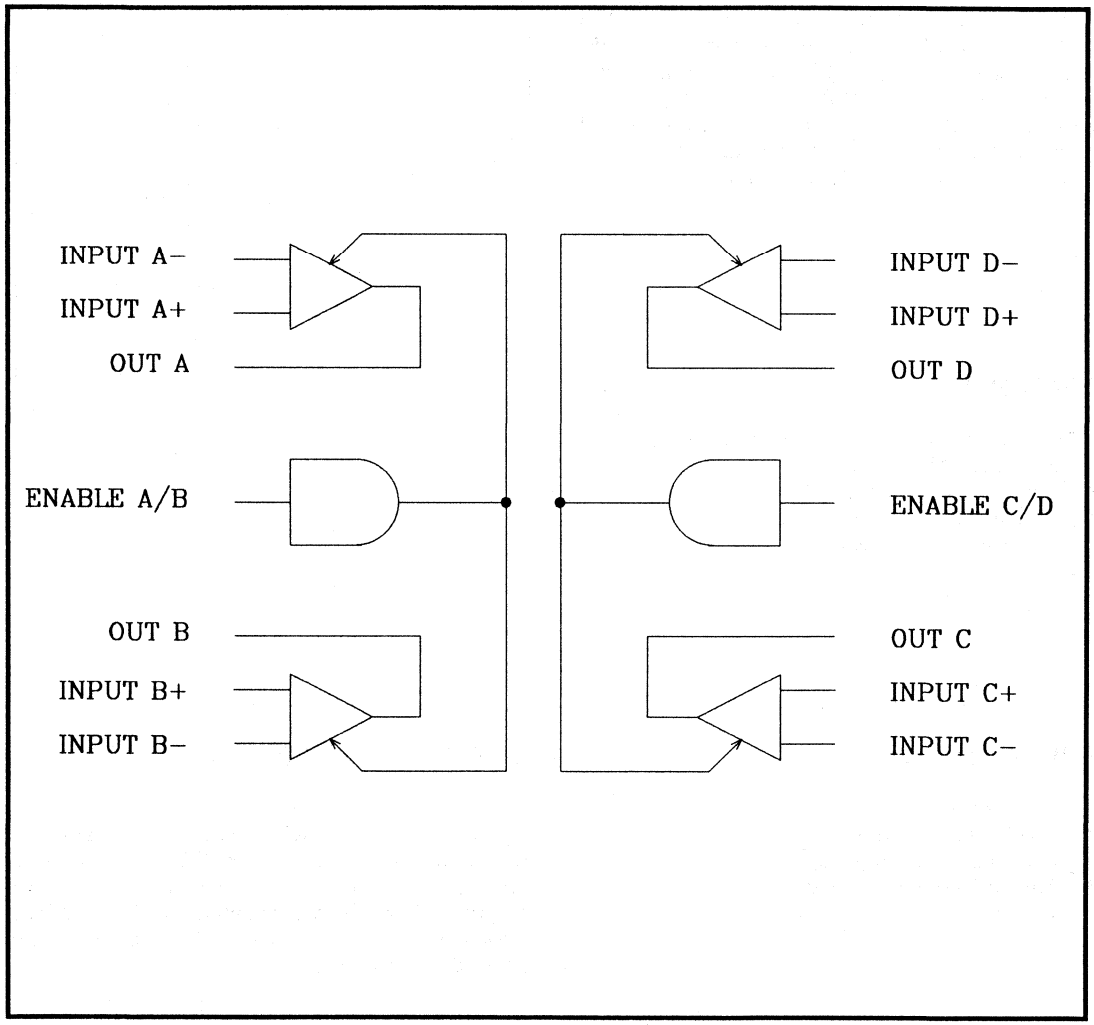
GENERAL DESCRIPTION

The ST34C86 is a high speed line receiver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C86CP16	Plastic	0° C to + 70° C
ST34C86CJ18	PLCC	0° C to + 70° C

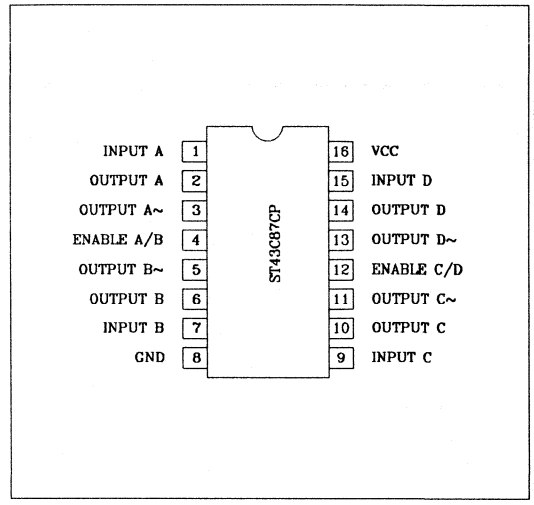
BLOCK DIAGRAM



QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST34C87 is a CMOS quad differential line driver,designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signal special hysteresis is built in the ST34C87 circuit.



FEATURES

* Pin-to-pin compatible with National DS34C87
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

APPLICATIONS

* Hard disk drives
* RS-422 controller cards
* MFM / RLL controller cards
* Digital line transmission driver

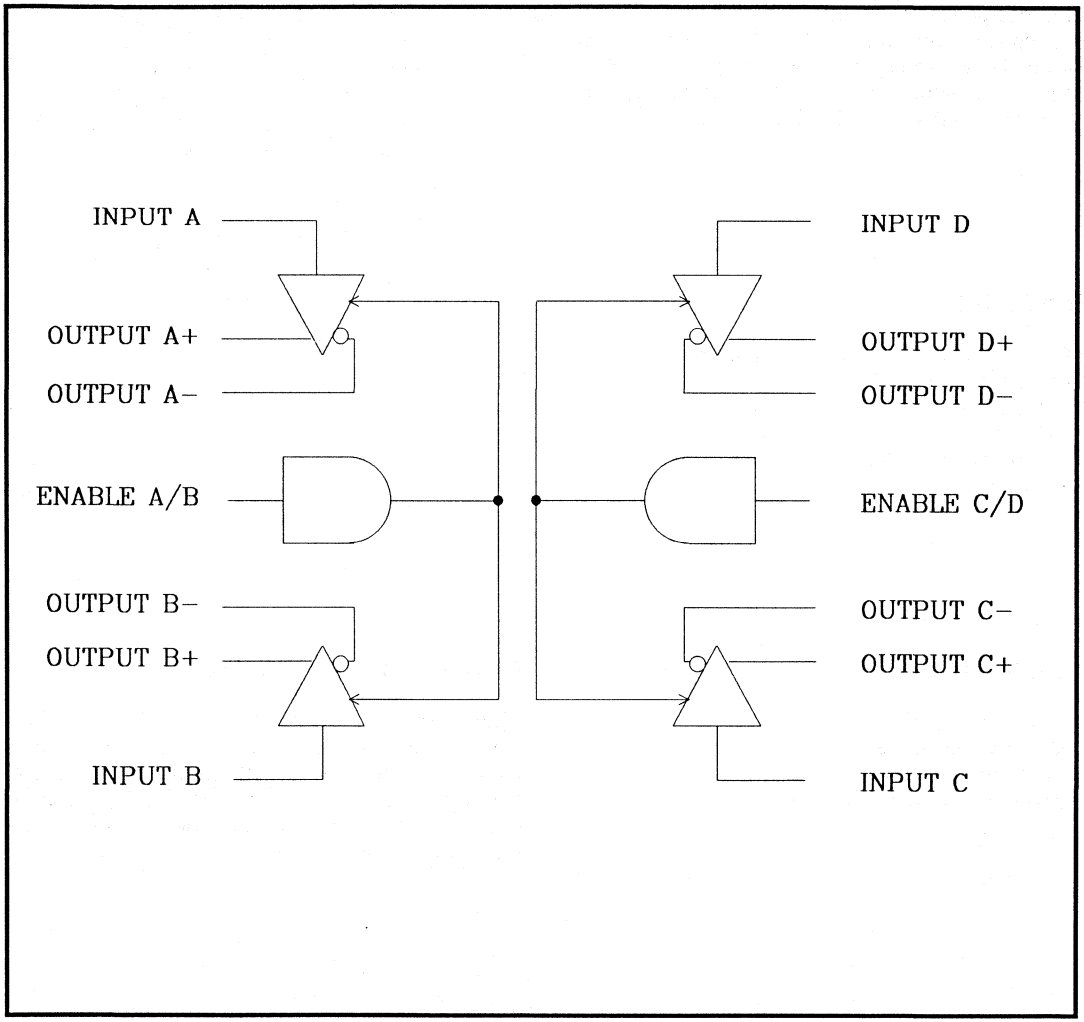
GENERAL DESCRIPTION

The ST34C87 is a high speed CMOS line driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C87CP16	Plastic	0° C to + 70° C
ST34C87CJ18	PLCC	0° C to + 70° C

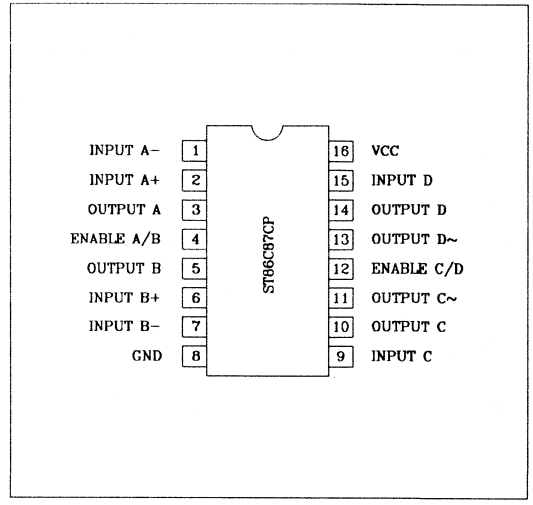
BLOCK DIAGRAM



DUAL RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER AND DRIVER

DESCRIPTION

The ST86C87 is a CMOS dual differential line receiver and driver,designed to meet the standard RS-422, RS-432 requirements and digital data transmission over balanced lines. The ST86C87 has an input sensitivity of 200mv over the common mode input voltage rage of +/- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST86C87 circuit.



FEATURES

* Half section of National DS34C86 and DS34C87
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed
* Dual line receiver with three state control
* Dual line driver with three state control

APPLICATIONS

* Hard disk drives
* RS-422 controller cards
* MFM / RLL controller cards
* Differential transmission receiver and driver

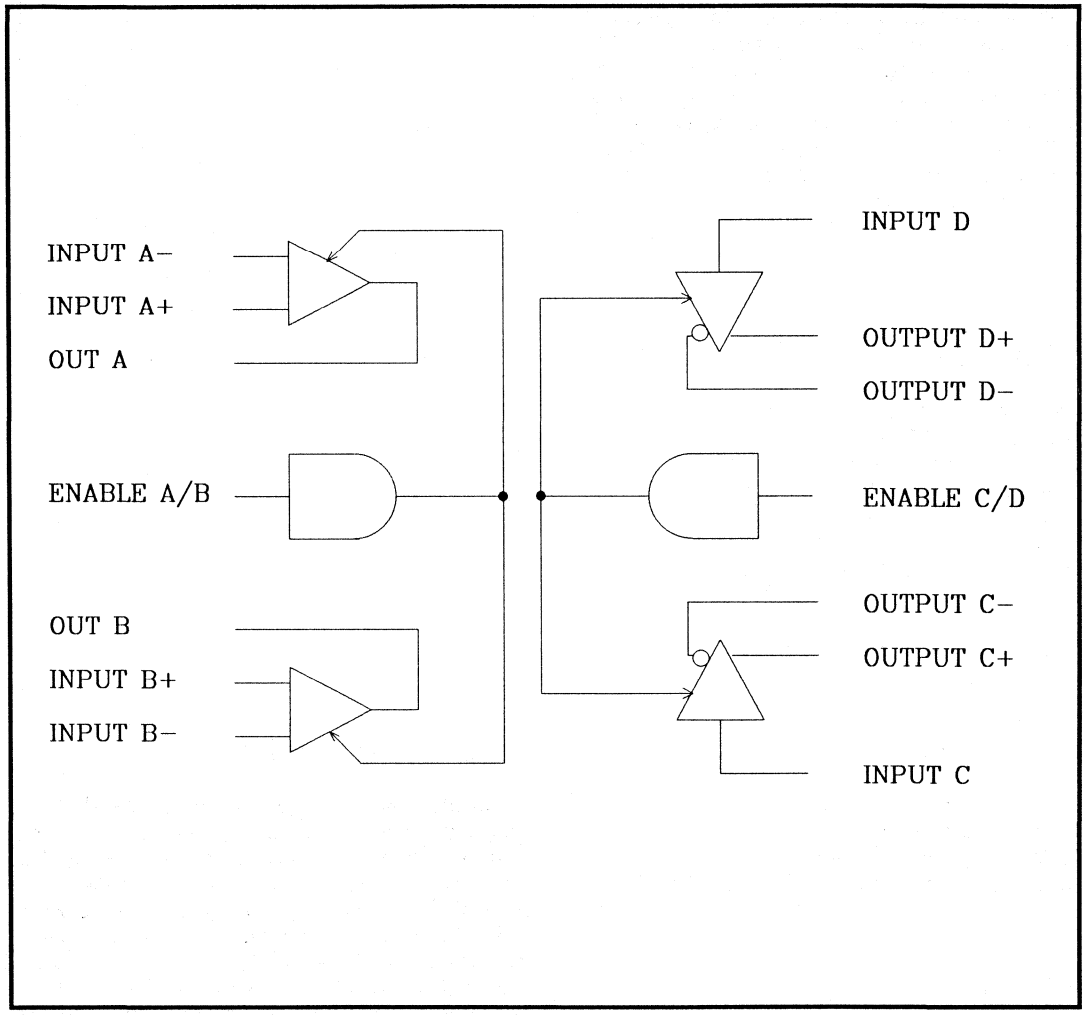
GENERAL DESCRIPTION

The ST86C87 is a high speed line receiver and driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS432 differential applications. ST86C87 provides TTL compatible outputs to interface with standard 74LS and CMOS design enviroments. ST86C87 is suitable for low power 5V operation with Min board space requirements. ST86C87 provides dual differential line receiver with three state control pin and dual line driver with three state control capability.

ORDERING INFORMATION

Part number	Package	Operationg temperature
ST86C87CP16	Plastic	0° C to + 70° C
ST86C87CJ18	PLCC	0° C to + 70° C

BLOCK DIAGRAM



MASS STORAGE

2

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UART

3

STARTECH

ST16C450

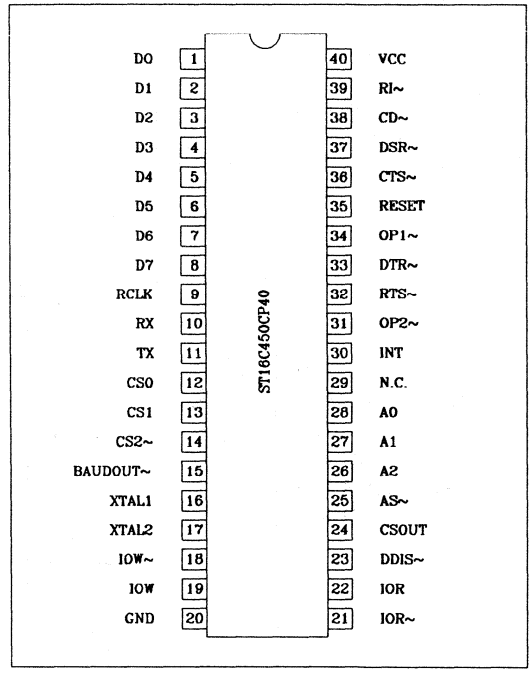
FEB 1991

ASYNCHRONOUS RECEIVER AND TRANSMITTER

3

DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C450 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Pin-to-pin and functionally compatible to INS8250, NS16C450
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.

APPLICATIONS

* Serial receiver or transmitter
* Serial to parallel/parallel to serial converter
* Modem with/without handshaking signals
* Terminal

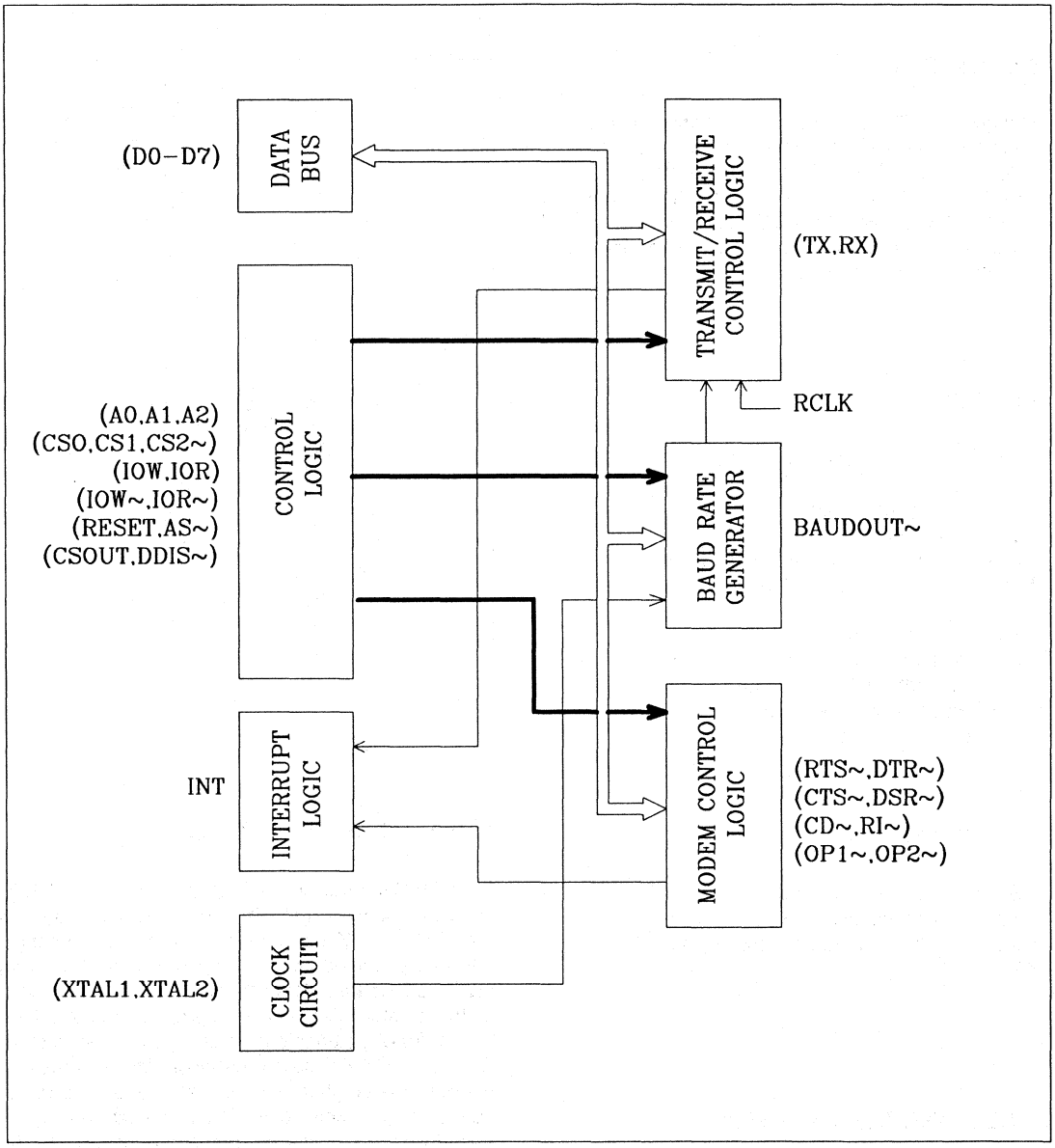
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C450CP40	Plastic	0° C to +70° C
ST16C450CJ44	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C450 is an improved version of the INS8250/NS16C450 UART with higher speed operating access time. The ST16C450 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status register will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C450 can interface easily to the most popular microprocessors, and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU . D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receiver clock input. The external clock input to the ST16C450 receiver section.
RX	10	I	Serial data input. The serial information received from MODEM or RS232 to ST16C450 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin (while CS1 = 1 and CS2 = 0) will enable the UART/CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin (while CS0 = 1 and CS2 = 0) will enable the UART/CPU data transfer operation.
CS2~	14	I	Chip select 3. (active low) A low at this pin (while CS0 = 1 and CS1 = 1) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe. (active high) Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to ST16C450 during write operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or GND(IOW = GND or IOW~ = VCC) .
GND	20	O	Signal and power ground.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
IOR~	21	I	Read strobe. (active low) A low level on this pin (while CS0 = 1, CS1 = 1 and CS2~ = 0) will transfer the contents of the ST16C450 data bus to the CPU.
IOR	22	I	Read strobe. (active high) Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from ST16C450 to CPU during read operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or GND (IOR = GND or IOR~ = VCC) .
DDIS~	23	O	Drive disable. (active low) This pin goes low when CPU is reading data from ST16C450 to disable the external transceiver or logics.
CSOUT	24	O	Chip select out. A high on this pin indicates that the chip has been selected by the chip select input pins.
AS~	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
OP2~	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register.
RTS~	32	O	Request to send. (active low) To indicate the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
DTR~	33	O	Data terminal ready. (active low) To indicate that ST16C450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
OP1~	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS~	36	I	Clear to send. (active low) The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
DSR~	37	I	Data set ready. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
CD~	38	I	Carrier detect. (active low) A low on this pin indicates that a carrier has been detected by the modem.
RI~	39	I	Ring detect indicator. (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTION

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register and Transmit Shift Register. The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of data bus (D7-D0) to the transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

ST16C450 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

INTERRUPT ENABLE REGISTER (IER)
The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)
The ST16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C450 provides the highest interrupt level to be serviced by CPU, no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR bit-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR bit-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TX) to go low to

alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB)
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER (MCR)
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
0=set OP1~ output to high
1=set OP1~ output to low

MCR BIT -3:
0=set OP2~ output to high
1=set OP2~ output to low

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (mark condition), the receiver input (RX) , CTS~, DSR~, CD~, and RI~ are disabled. Internally transmitter output is connected to the receiver input and DTR~, RTS~, OP1~, and OP2~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1= data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. ST16C450 will not accept any data for transmission
1=transmit holding register is empty. CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER (SR)
ST16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432MHz crystal or external clock)

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C450 RESET CONDITION TABLE

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
TX	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{10}	Chip select output delay from select			50	ns	100 pF load
T_{11}	IOR~ to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW~	5			ns	Note: 1
T_{13}	IOW~ delay from address	25			ns	Note: 1
T_{14}	IOW~ delay from chip select	10			ns	Note: 1
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	Note: 1
T_{21}	IOR~ delay from address	10			ns	Note: 1
T_{22}	IOR~ delay from chip select	10			ns	Note: 1
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	Note: 1
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		2^{16}-1		
T_4	Baud out negative edge delay			100	ns	100 pF load
T_4	Baud out positive edge delay			100	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when AS~ is tied low
* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

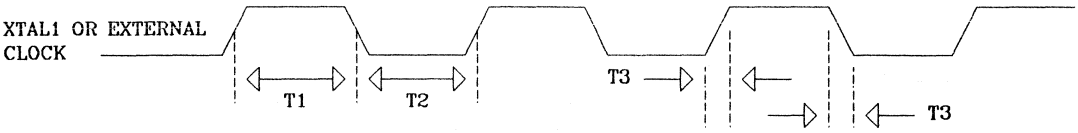
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

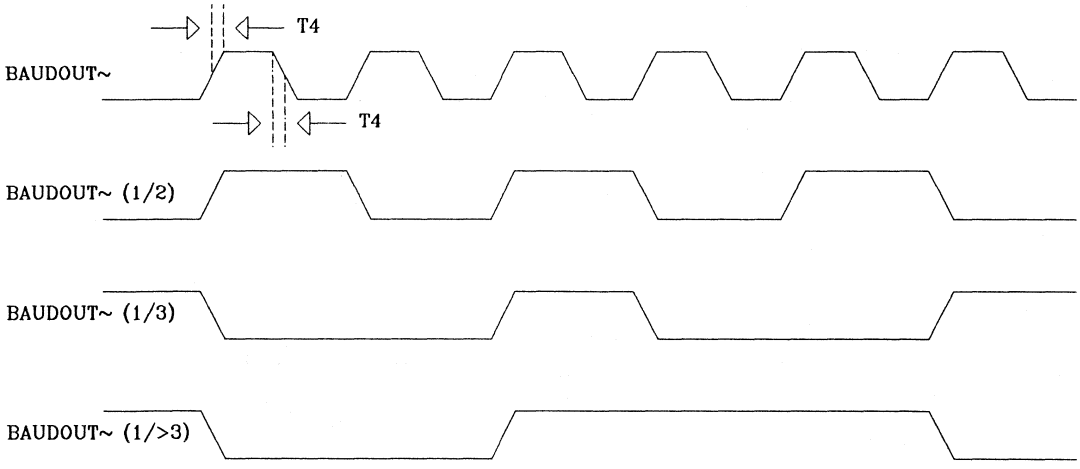
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

CLOCK TIMING

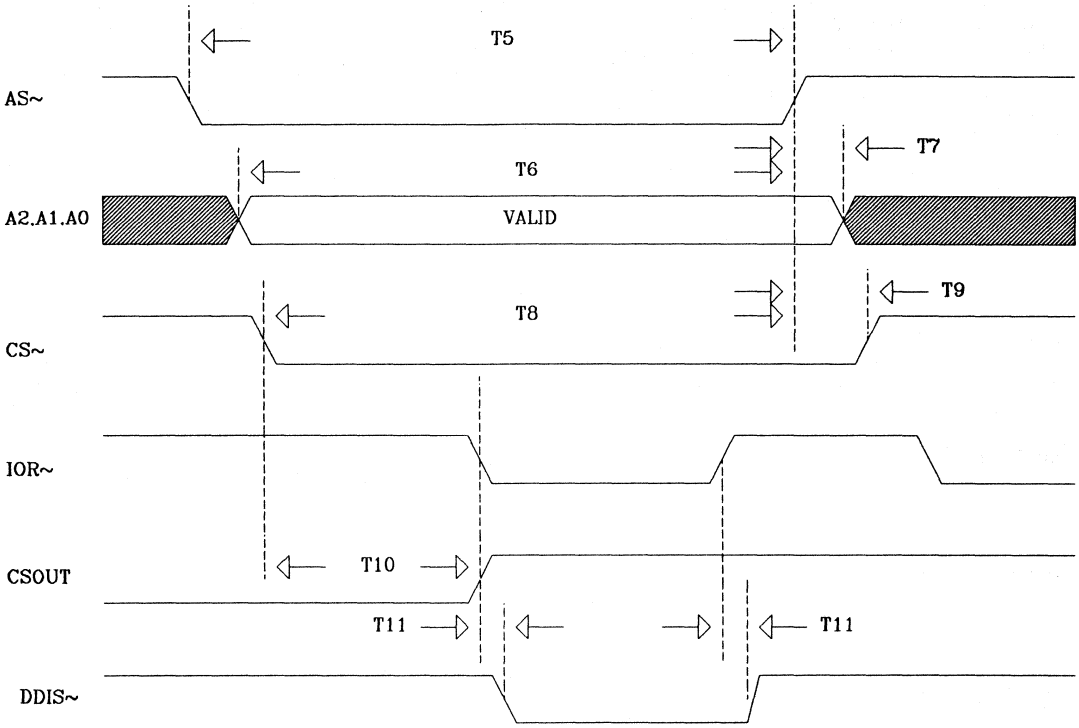


BAUDOUT~ TIMING



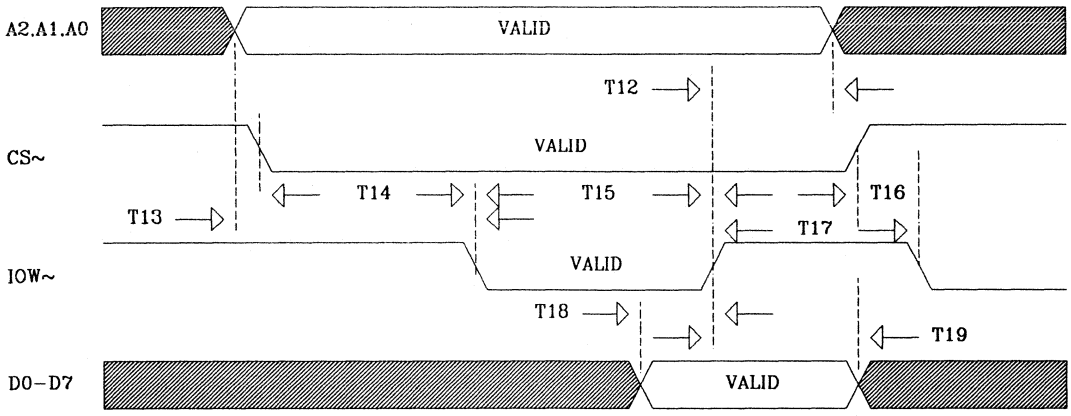
TIMING DIAGRAM

GENERAL TIMING

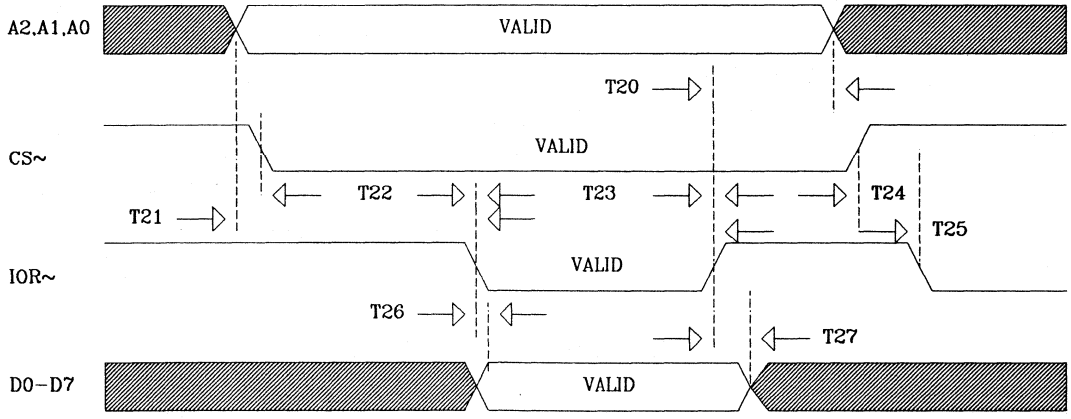


TIMING DIAGRAM

WRITE CYCLE TIMING

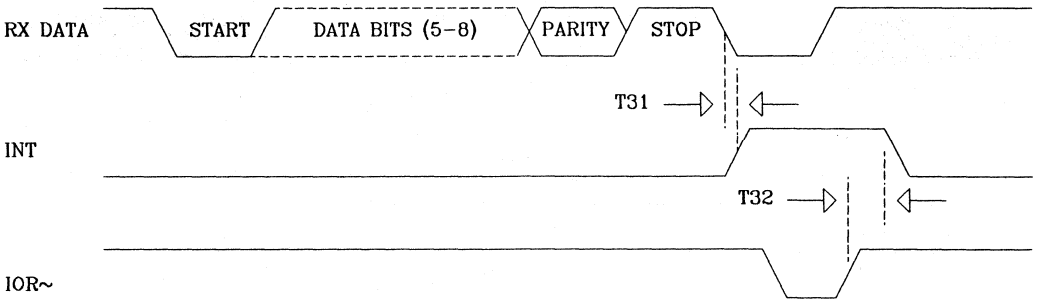


READ CYCLE TIMING

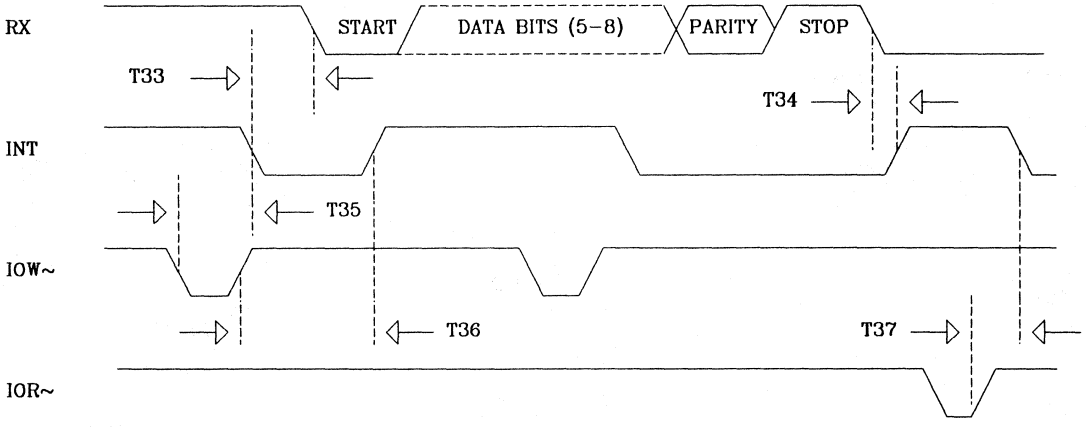


TIMING DIAGRAM

RECEIVER TIMING

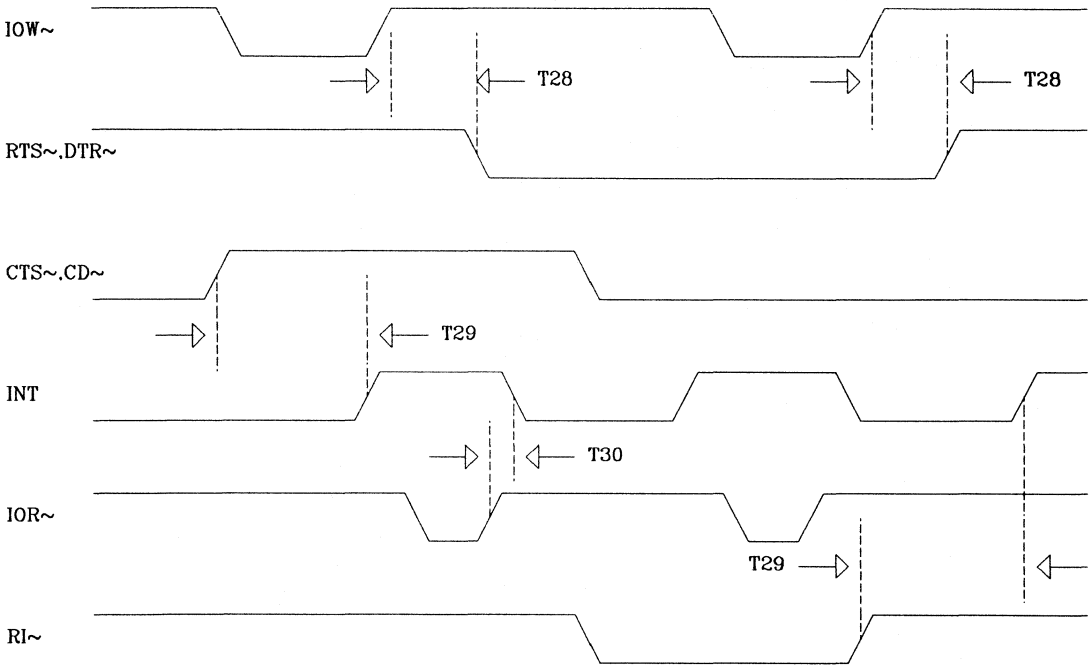


TRANSMITTER TIMING

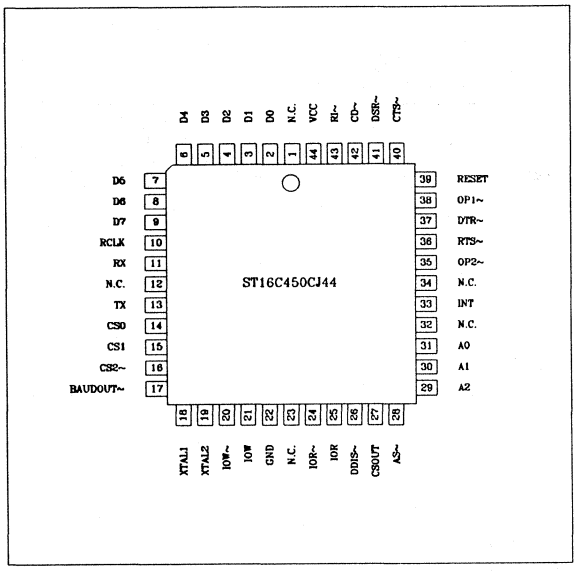


TIMING DIAGRAM

MODEM TIMING



44 pin PLCC pinout



STARTECH

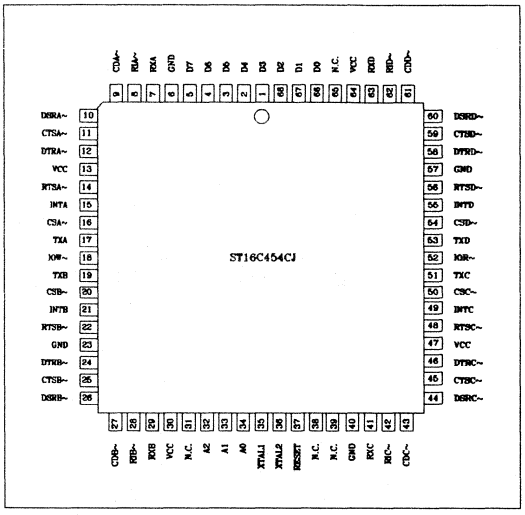
ST16C454

FEB 1991

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C454 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Quad ST16C450
* Pin-to-pin compatible to ST16C554
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs

APPLICATIONS

* Quad serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* Fax
* Terminals

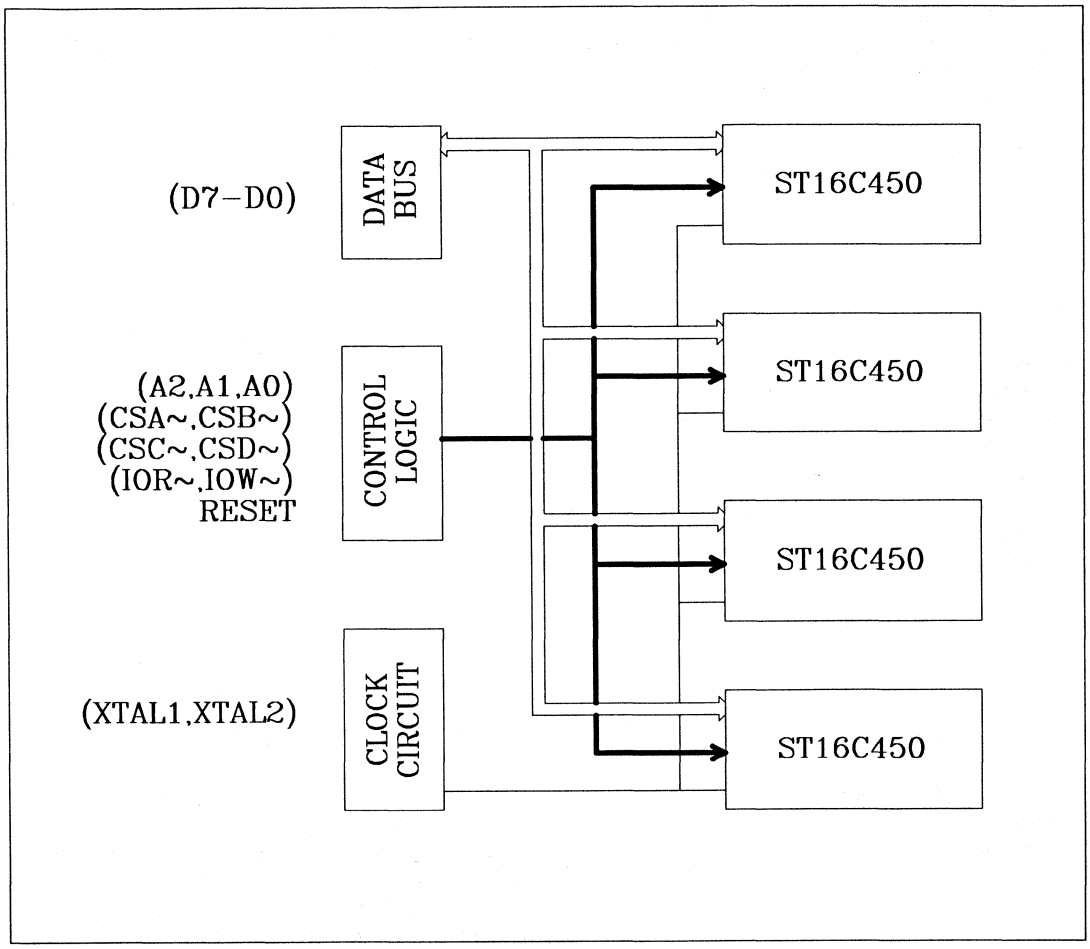
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C454CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C454 is an improved, quad version of the NS16450 UART with higher speed operating access time. The ST16C454 performs the parallel to serial/ serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C454 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	description
D7-D0	5-66	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST16C454 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B~ CS C-D~	16,20 50,54	I	Chip select A-D. (active low) A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
IOW~	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
CD A-B~ CD C-D~	9,27 43,61	I	Carrier detect A-D. (active low) A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23 40,57	O	Signal and power ground.
IOR~	52	I	Read strobe. (active low) A low level on this pin will transfer the contents of the ST16C454 data bus to the CPU.
DSR A-B~ DSR C-D~	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI A-B~ RI C-D~	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RTS A-B~ RTS C-D~	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A-B~ CTS C-D~	11,25 45,59	I	Clear to send A-D. (active low) The CTS~ signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
INT A-B INT C-D	15,21 49,55	O	Interrupt output A-D. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR A-B~ DTR C-D~	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST16C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT A-D output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST16C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C454 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	0	0	0	LSR A-D (Receiver Line Status Register)
2	0	0	0	RXRDY A-D (Received Data Ready)
3	0	0	0	TXRDY A-D (Transmitter holding register empty)
4	0	0	0	MSR A-D (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR BIT-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TX A-D) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0 = force RTS~ output to high
1 = force RTS~ output to low

MCR BIT-2:
x = not used

MCR BIT -3:
0 = Disable the INT output
1 = Enable the INT output

MCR BIT -4:
0 = normal operating mode
1 = enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D~, DSR A-D~, CD A-D~, and RI A-D~) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D~, RTS A-D~ and OP A-D~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0 = no data in receive holding register
1 = a data has been received and saved in the receive holding register

LSR BIT-1:
0 = no overrun error (normal)
1 = overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0 = no parity error (normal)
1 = parity error, received data does not have correct parity information

LSR BIT-3:
0 = no framing error (normal)
1 = framing error received, received data did not have a valid stop bit

LSR BIT-4:
0 = no break condition (normal)
1 = receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0 = transmit holding register is full; ST16C454 will not accept any data for transmission
1 = transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0 = transmitter holding and shift registers are full
1 = transmitter holding and shift registers are empty

LSR BIT-7:
This bit is not used and is set to zero.

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C454 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C454 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to ST16C450-OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to ST16C450-OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A-D
ST16C454 provides a temporary data register to store 8 bits of information for variable use.

ST16C454 EXTERNAL RESET CONDITION

REGIISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7=input signal

SIGNALS	RESET STATE
TX A-D	High
OP A-D~	High
RTS A-D~	High
DTR A-D~	High

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86
112K	1	

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
200	2304	
300	1536	
600	768	
1200	384	
2400	192	
4800	96	
9600	48	
19.2K	24	
28.8K	16	
38.4K	12	
76.8K	6	
153.6K	3	
224K	2	2.86
448K	1	

ST16C454 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

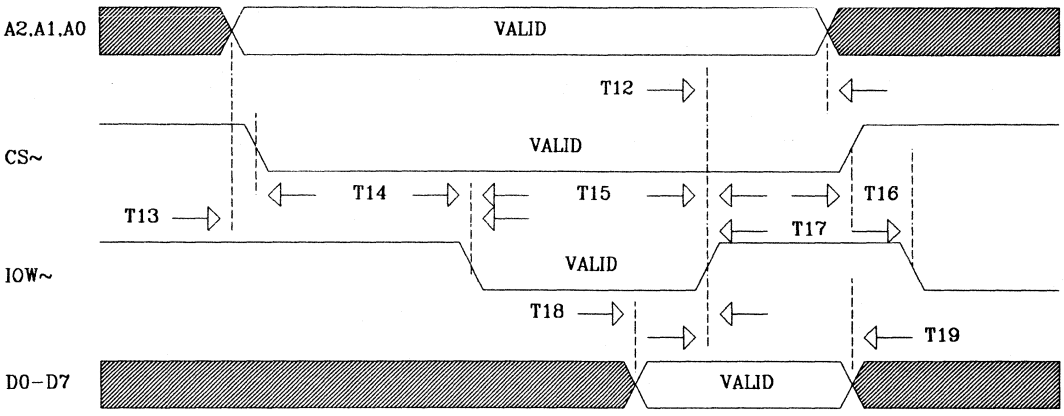
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

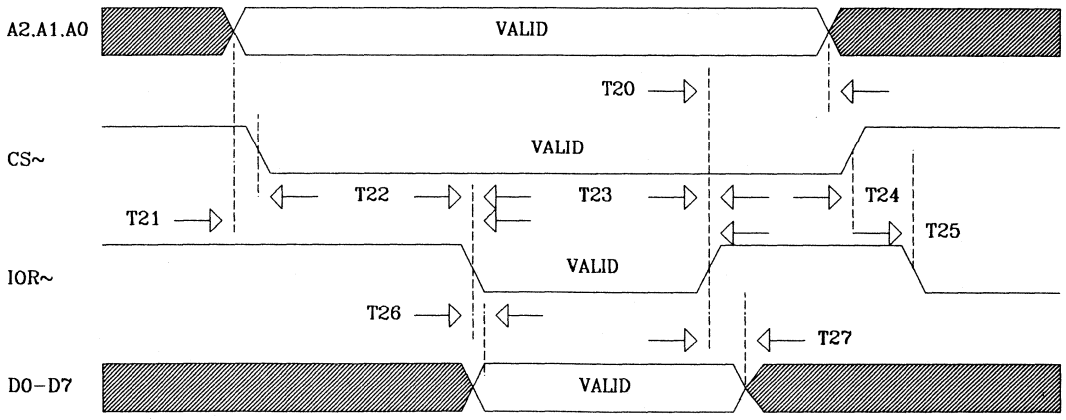
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

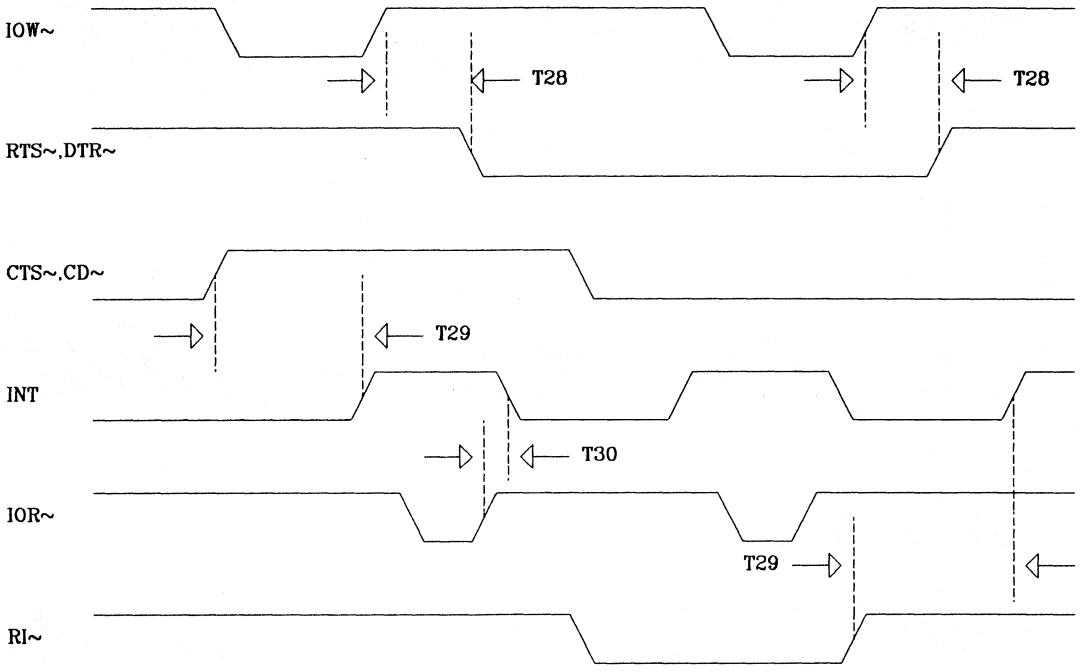


READ CYCLE TIMING



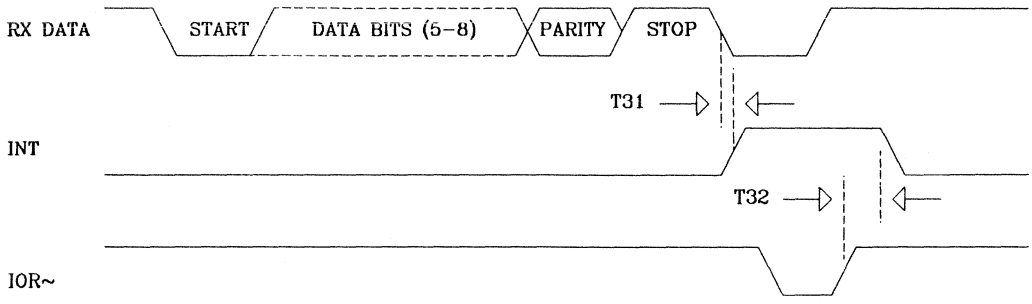
TIMING DIAGRAM

MODEM TIMING

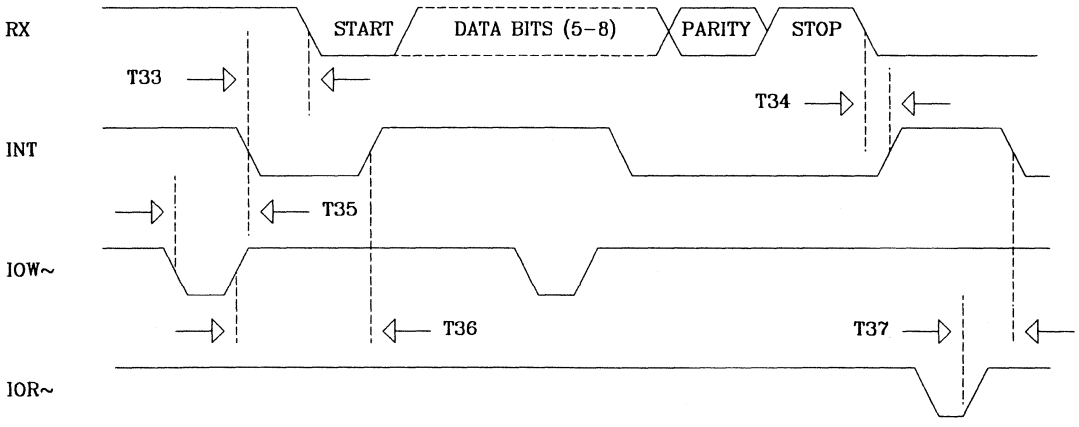


TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



STARTECH

ST16C550

MAY 1991

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

3

DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with FIFO and modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C550 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.

FEATURES

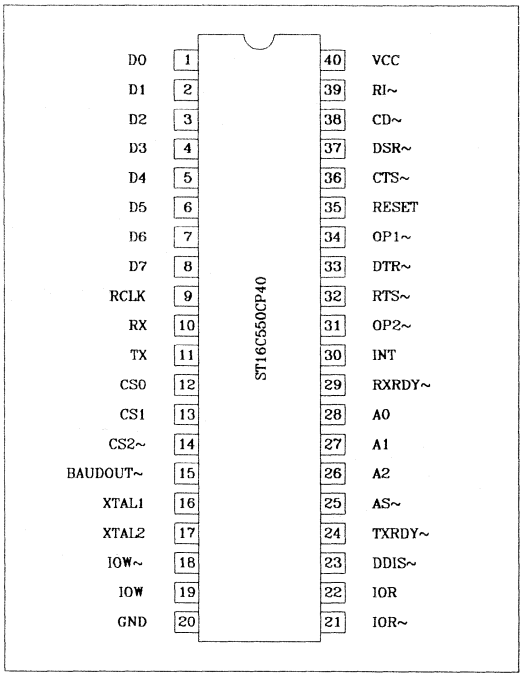
*Pin to pin and functional compatible to NS16550,VL16C550,WD16C550
*16 byte transmit FIFO
*16 byte receive FIFO with error flags
*Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
*Programmable character lengths (5, 6, 7, 8)
*Even, odd, or no parity bit generation and detection
*Status report register
*Independent transmit and receive control
*TTL compatible inputs, outputs
*Software compatible with INS8250, NS16C450
*448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

APPLICATIONS

* Serial receiver or transmitter
* Serial to parallel/parallel to serial converter
* Modem handshaking
* IBM PS/2 serial port
* Fax

ORDERING INFORMATION

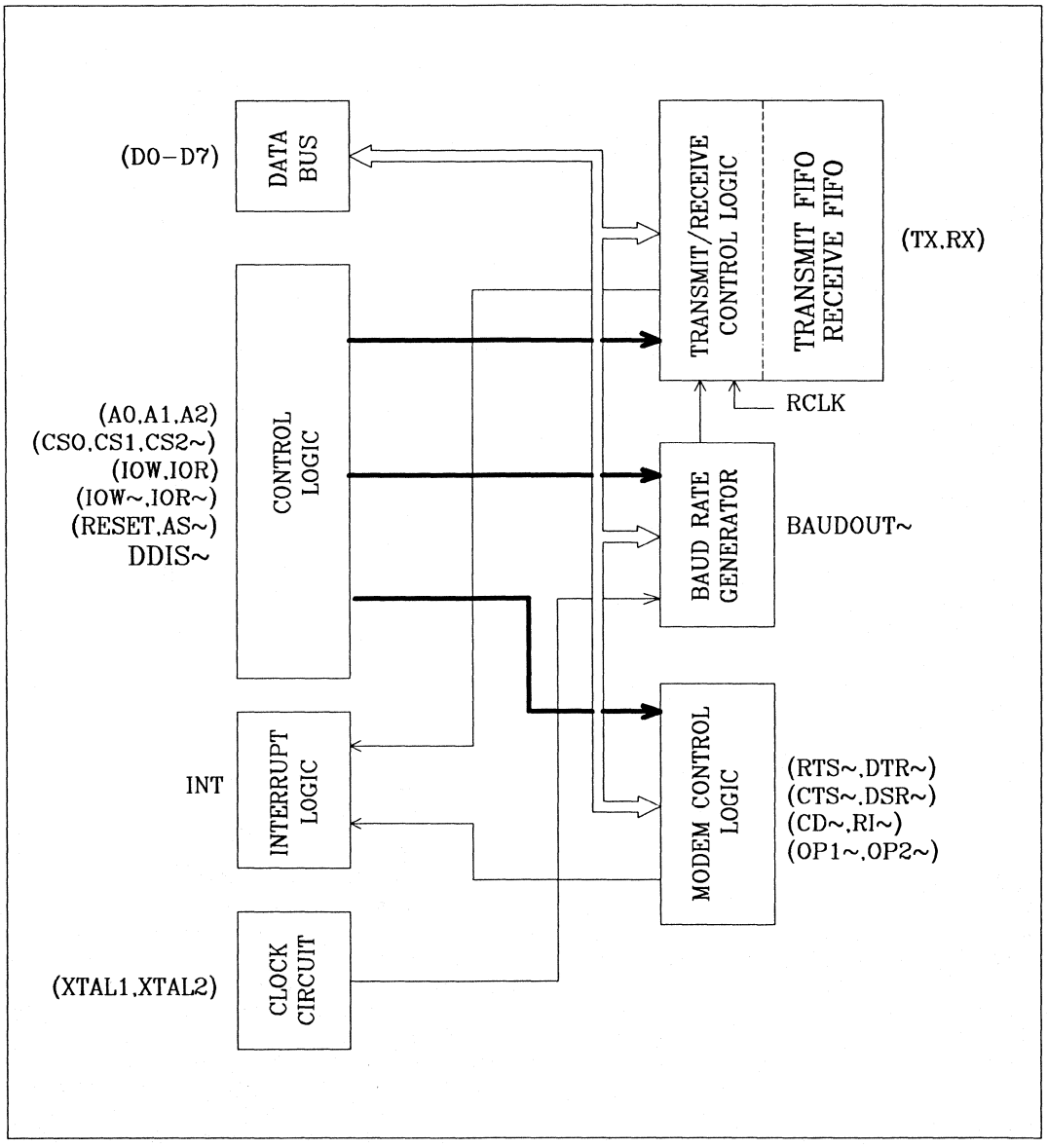
Part number	Package	Operating temperature
ST16C550CP40	Plastic	0° C to + 70° C
ST16C550CJ44	PLCC	0° C to + 70° C



GENERAL DESCRIPTION

The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. On board 16 byte (plus 3 bits of error data per byte in the RX-FIFO) FIFO and two DMA signaling functions are designed to minimize system overhead and maximize system efficiency.The ST16C550 provides internal loop-back capability for on board diagnostic testing.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the ST16C550 receiver section.
RX	10	I	Serial data input. The serial information (data) received from MODEM or RS232 to ST16C550 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin (while CS1 = 1 and CS2~ = 0) will enable the UART / CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin (while CS0 = 1 and CS2~ = 0) will enable the UART / CPU data transfer operation.
CS2~	14	I	Chip select 3. (active low) A low at this pin (while CS0 = 1 and CS1 = 1) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe. (active high) Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to ST16C550 during write operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or GND (IOW = GND or IOW~ = VCC) .

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
GND	20	O	Signal and power ground.
IOR~	21	I	I/O read strobe. (active low) A low level on this pin (while CS0=1, CS1=1 and CS2~=0) will transfer the contents of the ST16C550 data bus to the CPU.
IOR	22	I	Read strobe. (active high) Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from ST16C550 to CPU during read operation (while CS0=1, CS1=1 and CS2~=0). The unused pin should be tied to VCC or GND (IOR=GND or IOR~=VCC) .
DDIS~	23	O	Drive disable. (active low) This pin goes low when the CPU is reading data from the ST16C550 to disable the external transceiver or logics.
TXRDY~	24	O	Transmit ready. (active low) This pin goes low when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer DMA.
AS~	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS~ input permanently low.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
RXRDY~	29	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer DMA.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2~	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register.
RTS~	32	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTR~	33	O	Data terminal ready. (active low) To indicate that ST16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
OP1~	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS~	36	I	Clear to send. (active low) The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
DSR~	37	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART.
CD~	38	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI~	39	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

ST16C550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

3

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout~ is equal to 16X of transmission baud rate (Baudout~=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1 = no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0 = No change.
1 = Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0 = No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0 = No change.
1 = Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	World length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high.
1=force DTR~ output to low.

MCR BIT-1:
0=force RTS~ output to high.
1=force RTS~ output to low.

MCR BIT-2:
0=set OP1~ output to high.
1=set OP1~ output to low.

MCR BIT-3:
0=set OP2~ output to high.
1=set OP2~ output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS~, DSR~, CD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OP1~ and OP2~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0 = no data in receive holding register or FIFO.
1 = data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0 = no overrun error (normal).
1 = overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0 = no parity error (normal).
1 = parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0 = no framing error (normal).
1 = framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0 = no break condition (normal).
1 = receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0 = transmit holding register is full. ST16C550 will not accept any data for transmission.
1 = transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0 = transmitter holding and shift registers are full.
1 = transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0 = Normal.
1 = At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD~ input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low
RXRDY~	High
TXRDY~	High

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR~ to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW~	5			ns	Note: 1
T_{13}	IOW~ delay from address	25			ns	Note: 1
T_{14}	IOW~ delay from chip select	10			ns	Note: 1
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	Note: 1
T_{21}	IOR~ delay from address	10			ns	Note: 1
T_{22}	IOR~ delay from chip select	10			ns	Note: 1
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	Note: 1
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		2^{16}-1		
T_4	Baud out negative edge delay			100	ns	100 pF load
T_4	Baud out positive edge delay			100	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when AS~ is tied low
* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

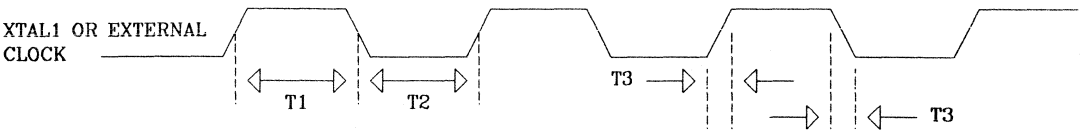
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

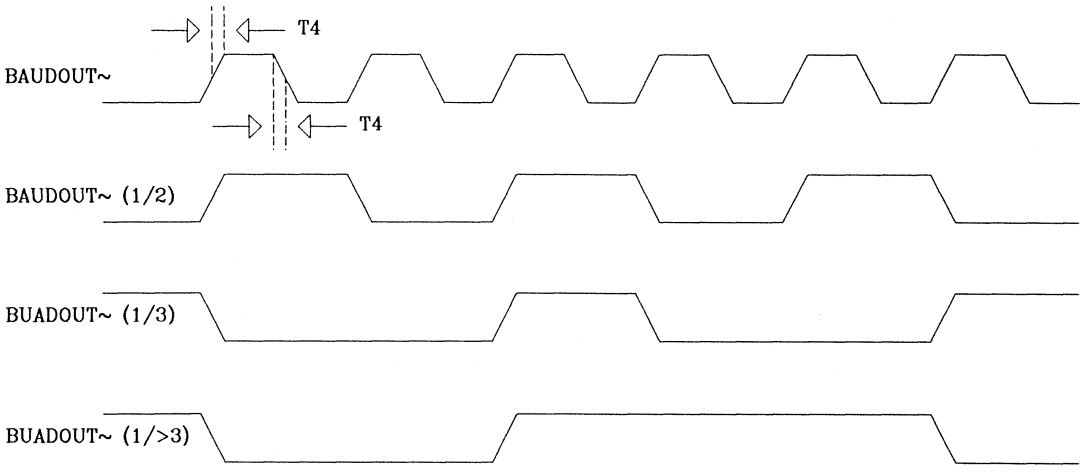
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

CLOCK TIMING

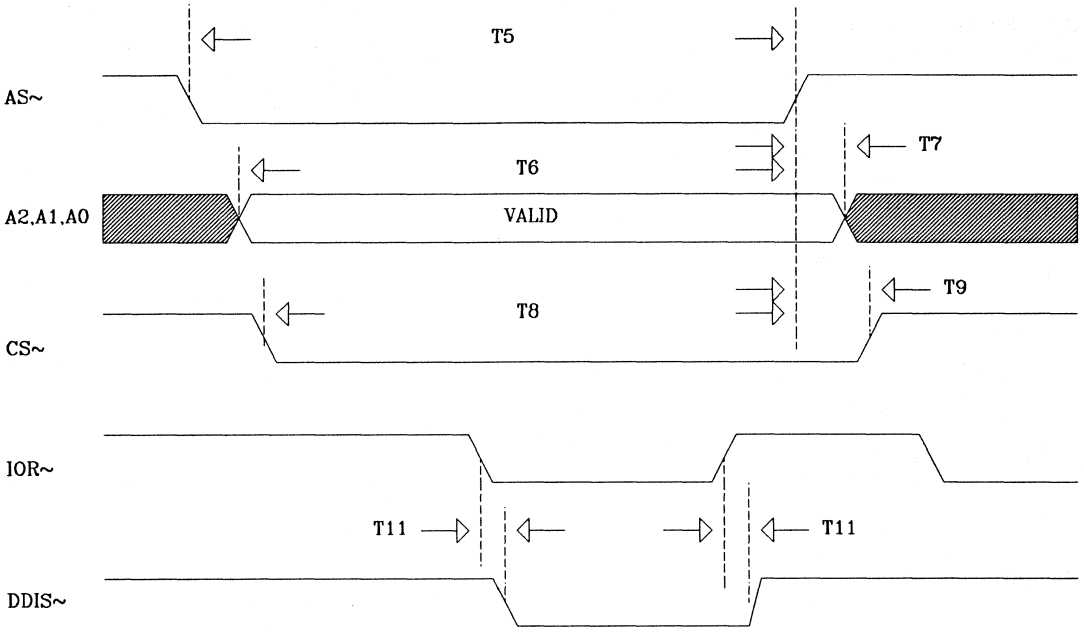


BAUDOUT~ TIMING



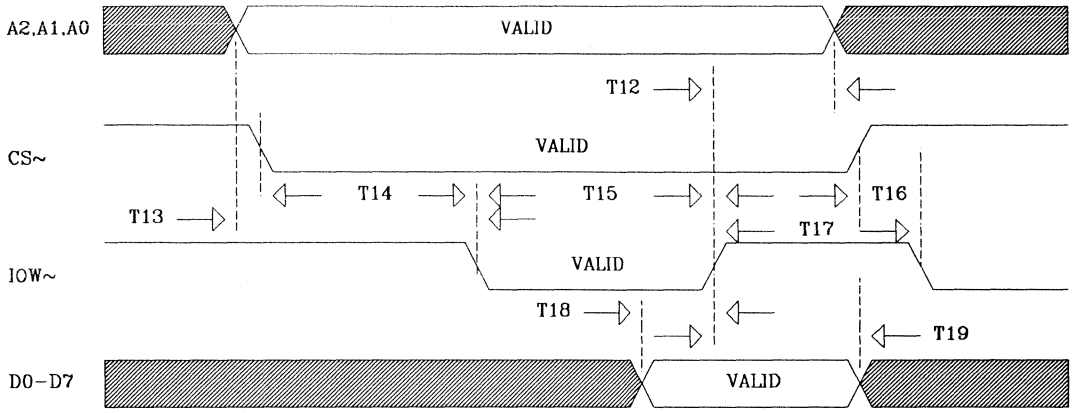
TIMING DIAGRAM

GENERAL TIMING

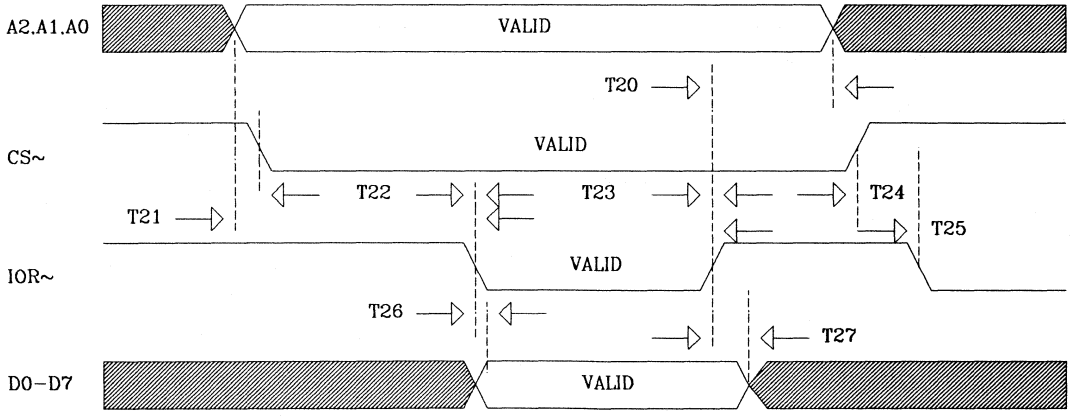


TIMING DIAGRAM

WRITE CYCLE TIMING

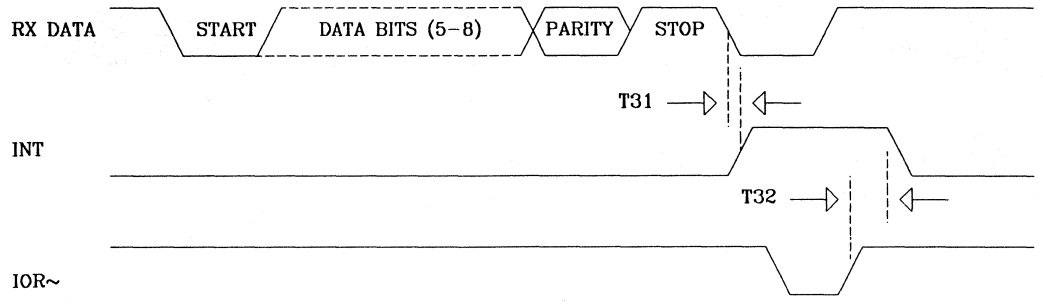


READ CYCLE TIMING

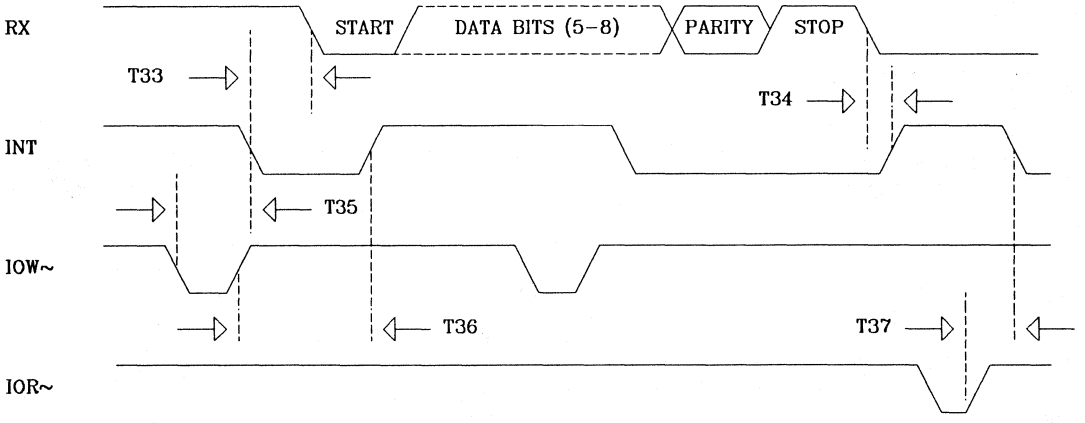


TIMING DIAGRAM

RECEIVER TIMING

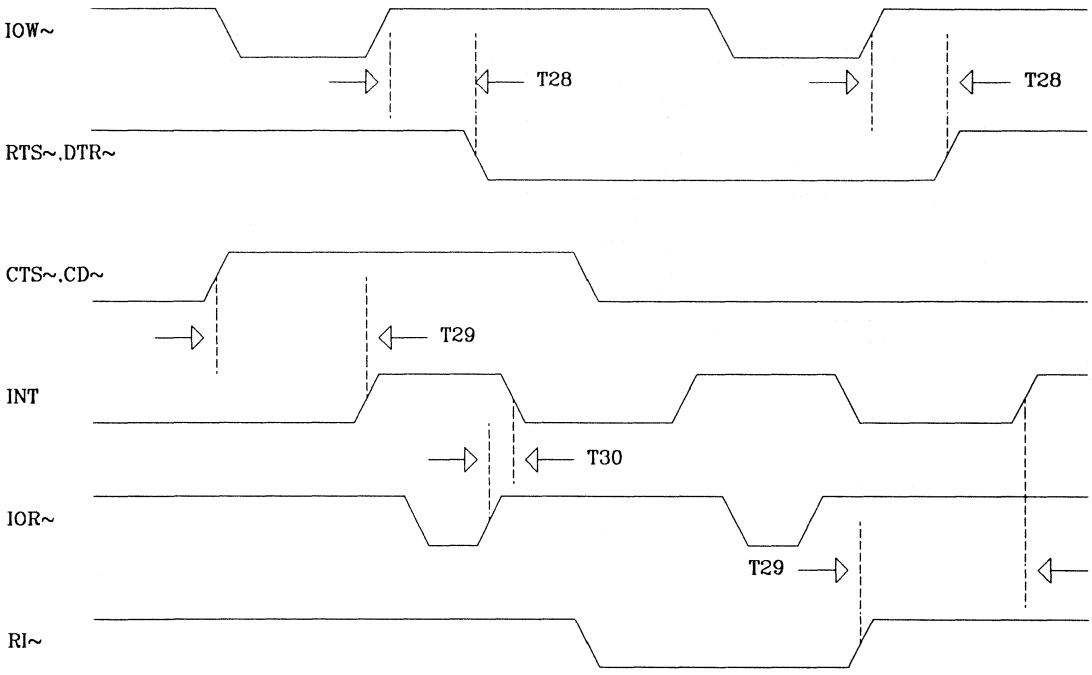


TRANSMITTER TIMING

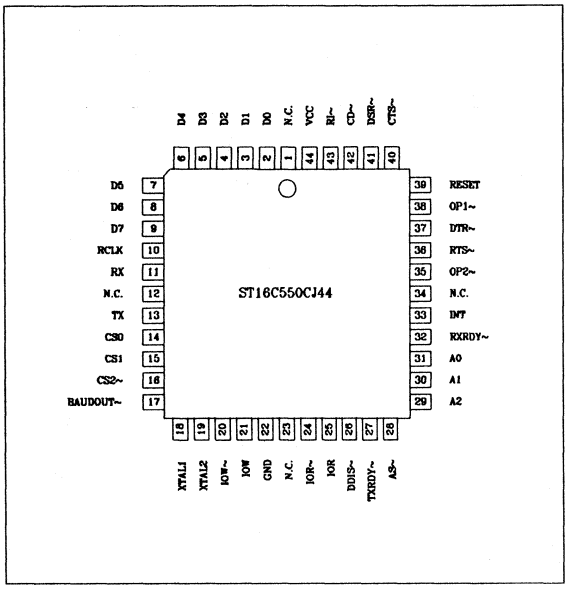


TIMING DIAGRAM

MODEM TIMING



44 Pin PLCC pinout



STARTECH

ST16C554

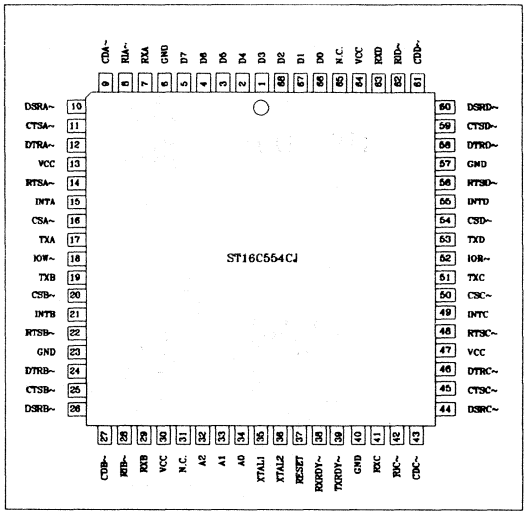
MAY 1991

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

3

DESCRIPTION

The ST16C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C554 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Quad ST16C550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz external clock source

APPLICATIONS

* Quad serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* Fax
* Terminals

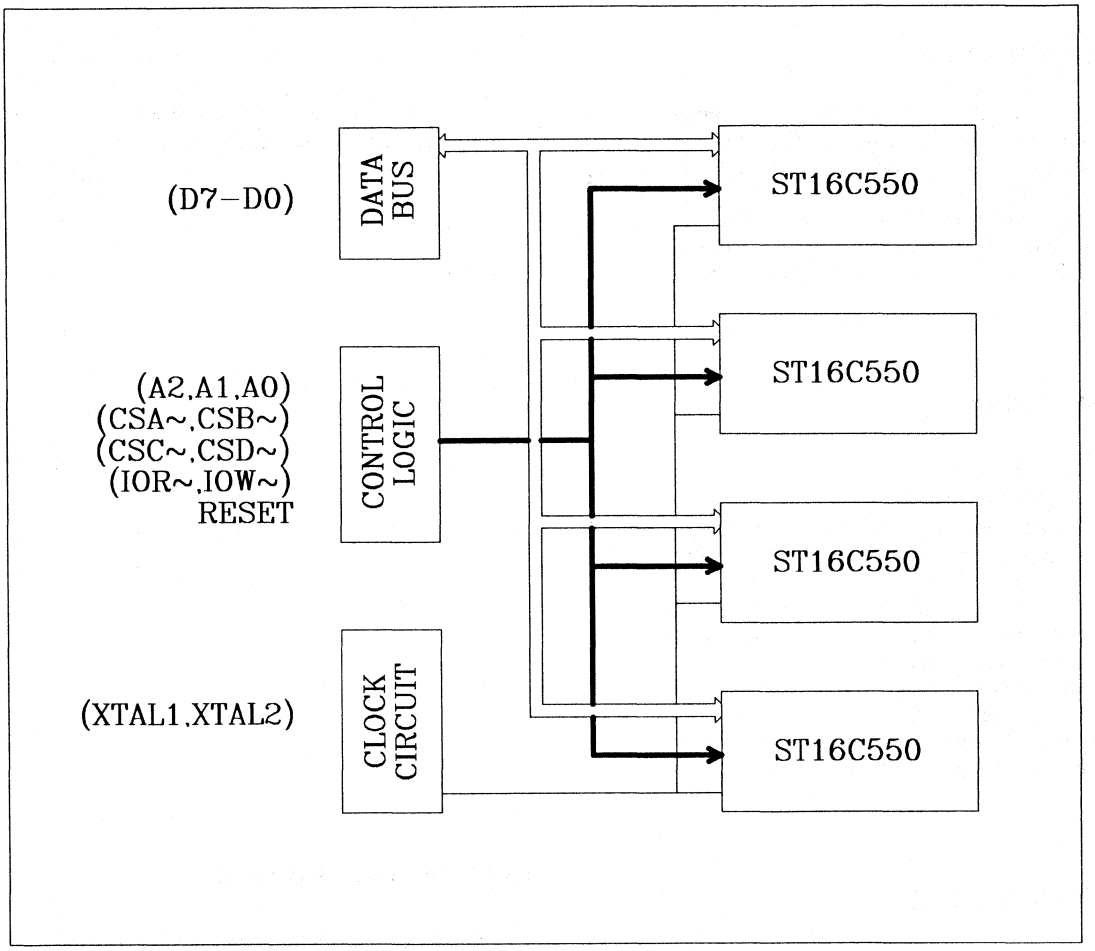
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C554 is an improved, quad version of the NS16550 UART with higher speed operating access time. The ST16C554 performs the parallel to serial/ serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C554 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	description
D7-D0	5-66	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST16C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B~ CS C-D~	16,20 50,54	I	Chip select A-D. (active low) A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
IOW~	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
CD A-B~ CD C-D~	9,27 43,61	I	Carrier detect A-D. (active low) A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23 40,57	O	Signal and power ground.
IOR~	52	I	Read strobe. (active low) A low level on this pin will transfer the contents of the ST16C554 data bus to the CPU.
DSR A-B~ DSR C-D~	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI A-B~ RI C-D~	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RTS A-B~ RTS C-D~	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A-B~ CTS C-D~	11,25 45,59	I	Clear to send A-D. (active low) The CTS~ signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
INT A-B INT C-D	15,21 49,55	O	Interrupt output A-D. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR A-B~ DTR C-D~	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.
TXRDY~	39	O	Transmit ready (active low). This pin goes low when the transmit FIFO of the ST16C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY~	38	O	Receive ready (active low). This pin goes low when the receive FIFO of the ST16C554 is full. It can be used as a single or multi-transfer DMA.

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
B) LSR BIT4-1 will specify which error(s) has occurred.
C) LSR BIT-5 will indicate when the transmit FIFO is empty.
D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D
The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT A-D output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C554 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	0	0	0	LSR A-D (Receiver Line Status Register)
2	0	0	0	RXRDY A-D (Received Data Ready)
3	0	0	0	TXRDY A-D (Transmitter holding register empty)
4	0	0	0	MSR A-D (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7**: are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0 = No change.
1 = Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0 = No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0 = No change.
1 = Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR BIT-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TX A-D) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0=Disable the INT output
1=Enable the INT output

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D~, DSR A-D~, CD A-D~, and RI A-D~) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D~, RTS A-D~ and OP A-D~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST16C554 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to ST16C550-OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to ST16C550-OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A-D
ST16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C554 EXTERNAL RESET CONDITION

REGIISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7=input signals

SIGNALS	RESET STATE
TX A-D	High
OP A-D~	High
RTS A-D~	High
DTR A-D~	High

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
200	2304	
300	1536	
600	768	
1200	384	
2400	192	
4800	96	
9600	48	
19.2K	24	
28.8K	16	
38.4K	12	
76.8K	6	
153.6K	3	
224K	2	2.86
448K	1	

ST16C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	OP1~	RTS~	DTR~
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

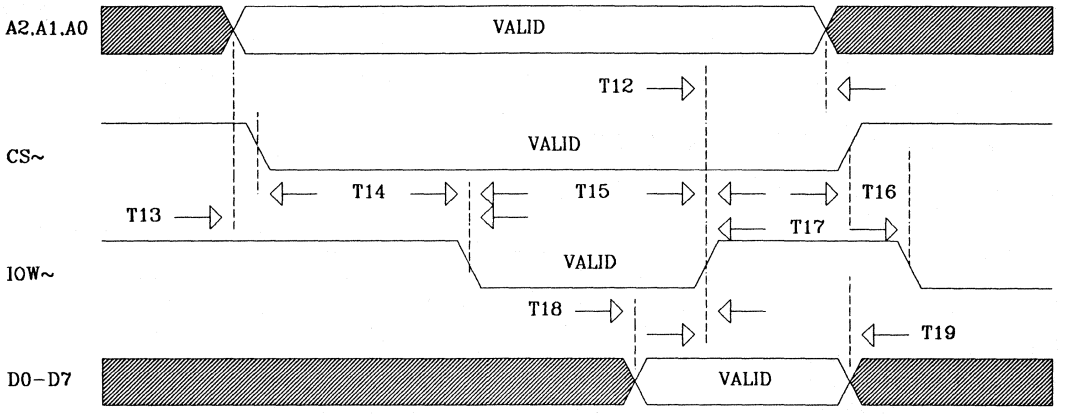
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

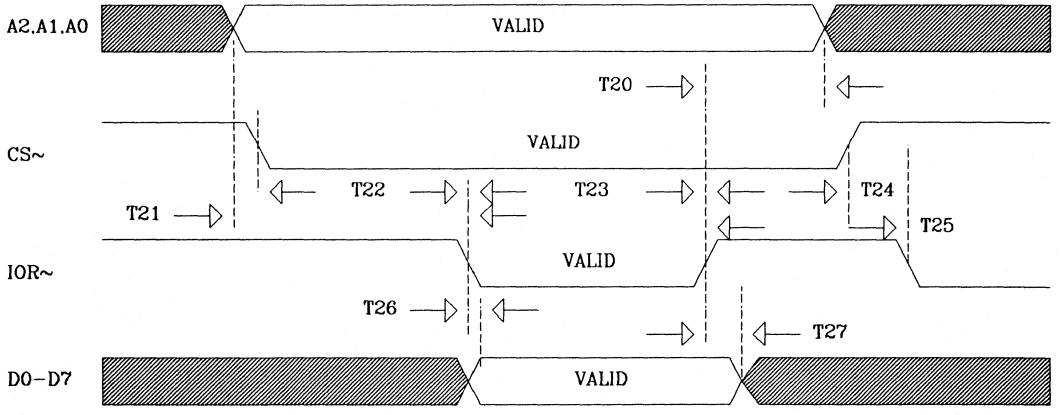
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

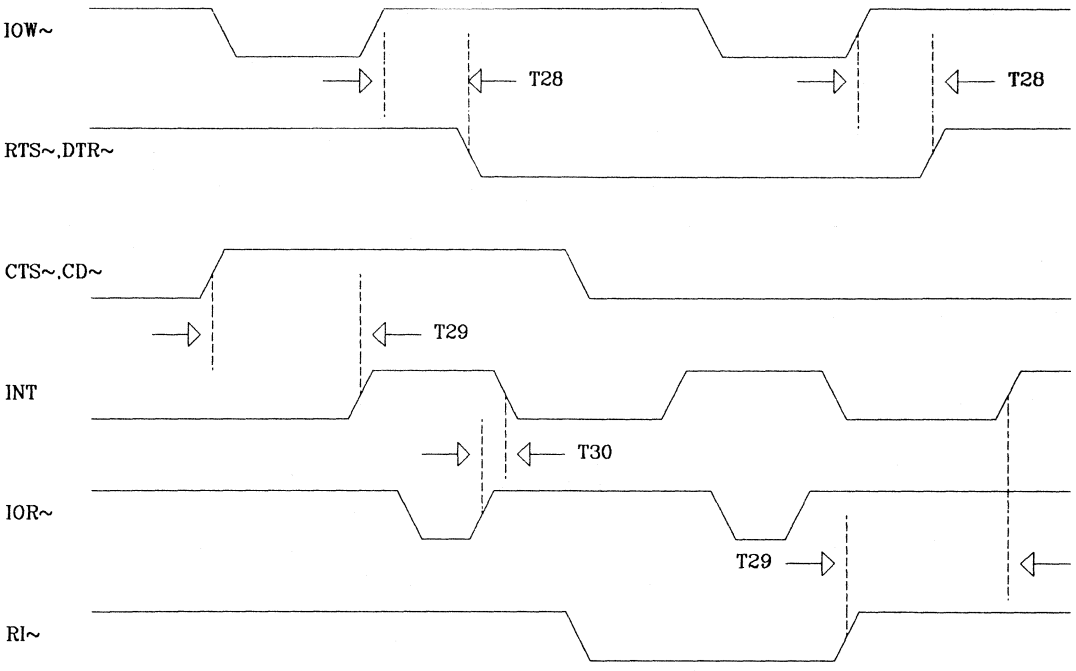


READ CYCLE TIMING



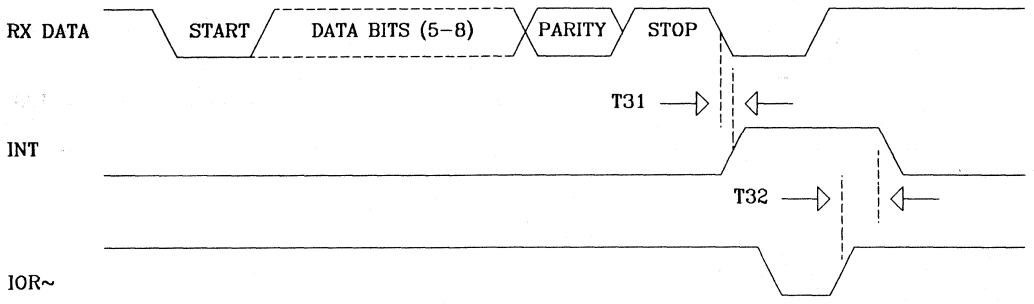
TIMING DIAGRAM

MODEM TIMING

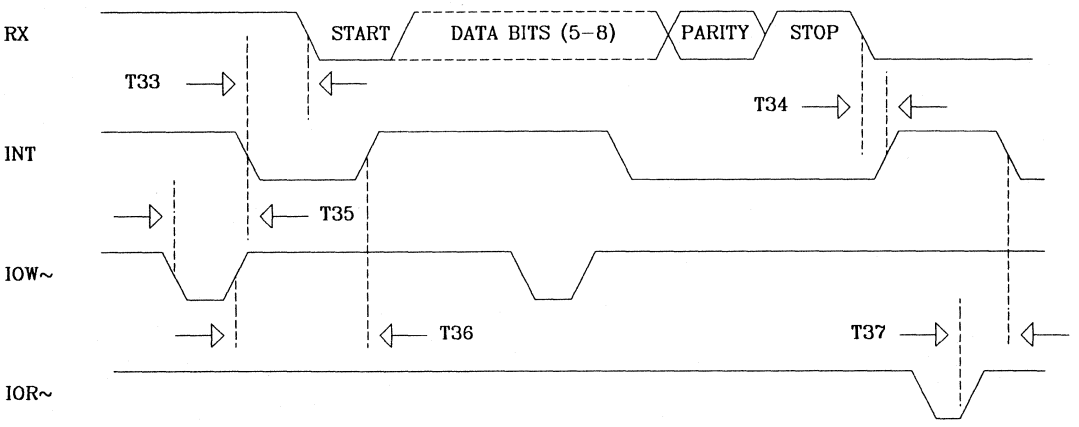


TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



STARTECH

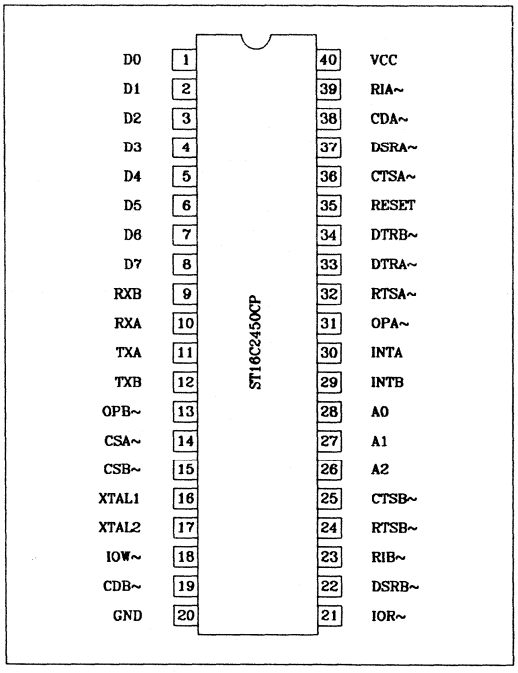
ST16C2450

FEB 1991

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C2450 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Dual ST16C450
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

APPLICATIONS

* Dual serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking

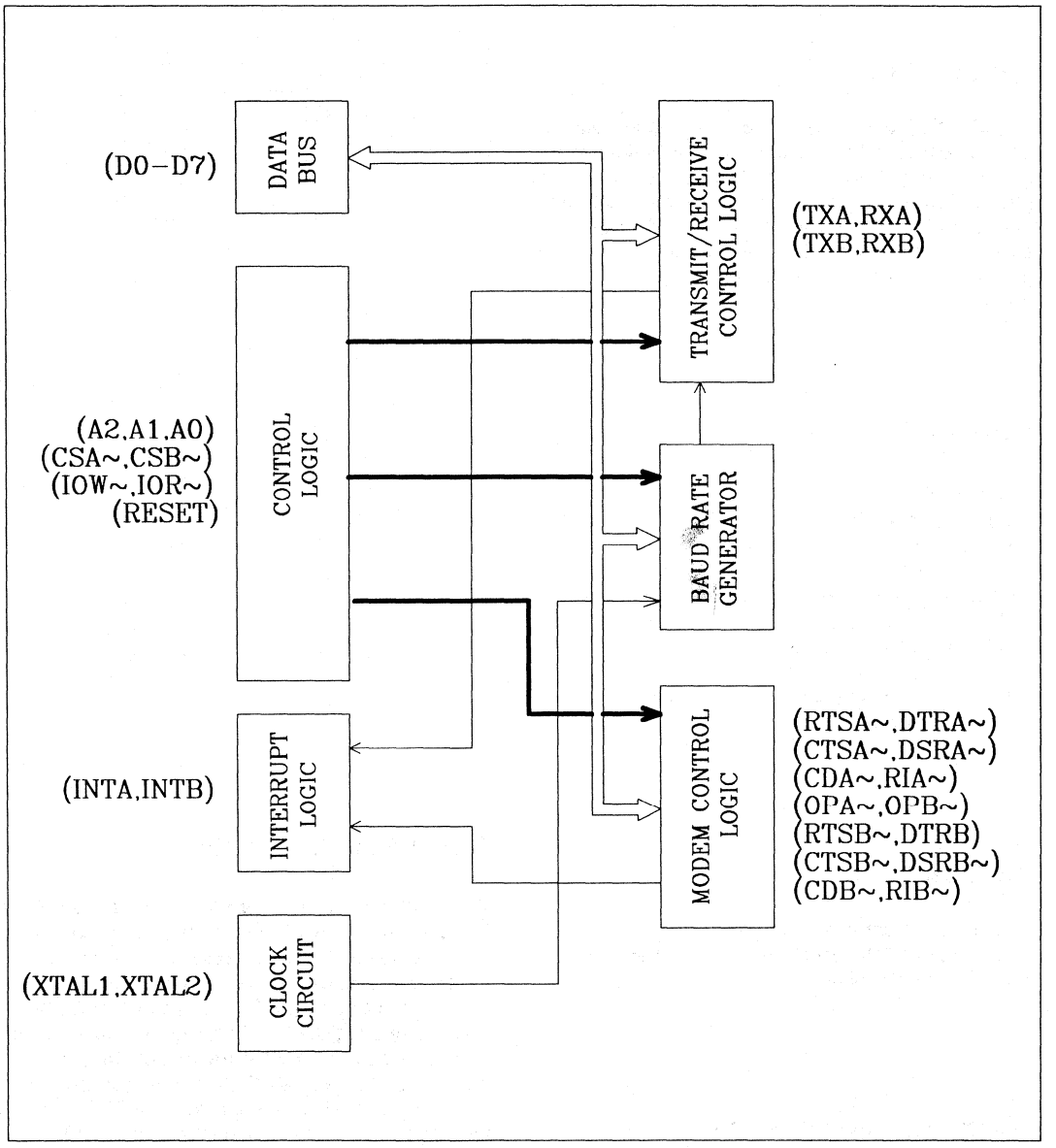
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2450CP40	Plastic	0° C to +70° C
ST16C2450CJ44	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C2450 is an improved, dual version of the INS8250/NS16C450 UART with higher speed operating access time. The ST16C2450 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C2450 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RXB	9	I	Serial data input B. The serial information received from MODEM or RS232 to ST16C2450 receive B circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally.
RXA	10	I	Serial data input A . The serial information received from MODEM or RS232 to ST16C2450 receive A circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXA input is disabled from external connection and connected to the TXA output internally.
TXA	11	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TXA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
TXB	12	O	Serial data output B. The serial data of channel B is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
OPB~	13	O	General purpose output. (active low) User defined output. See bit-3 modem control register B.
CSA~	14	I	Chip select A. (active low) A low at this pin will enable the UARTA/ CPU data transfer operation.
CSB~	15	I	Chip select B. (active low) A low at this pin will enable the UARTB/ CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
CDB~	19	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the modem B.
GND	20	O	Signal and power ground.
IOR~	21	I	I/O read strobe. (active low) A low level on this pin will transfer the contents of the ST16C2450 data bus to the CPU.
DSRB~	22	I	Data set ready B. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART B.
RIB~	23	I	Ring detect B indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTSB~	24	O	Request to send B. (active low) To indicate that transmitter B has data ready to send. Writing a "1" in the modem control register B (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	25	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INTB	29	O	Interrupt output B. (active high) This pin goes high (when enabled by the interrupt enable register B) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART B.
INTA	30	O	Interrupt output A. (active high) This pin goes high (when enabled by the interrupt enable register A) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A.
OPA~	31	O	General purpose output A. (active low) User defined output. See bit-3 modem control register A.
RTSA~	32	O	Request to send A. (active low) To indicate that transmitter A has data ready to send. Writing a "1" in the modem control register A (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTRA~	33	O	Data terminal ready A. (active low) To indicate that ST16C2450 (channel A) is ready to receive data. This pin can be controlled via the modem control register A (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
DTRB~	34	O	Data terminal ready B. (active low) To indicate that ST16C2450 (channel B) is ready to receive data. This pin can be controlled via modem control register B (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTSA~	36	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
DSRA~	37	I	Data set ready A. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART A.
CDA~	38	I	Carrier detect A. (active low) A low on this pin indicates that carrier has been detected by the modem A.
RIA~	39	I	Ring detect A indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
Vcc	40	I	Power supply input.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER A/B

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The ST16C2450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C2450 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	0	0	0	LSR A/B (Receiver Line Status Register)
2	0	0	0	RXRDY A/B (Received Data Ready)
3	0	0	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR BIT-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TXA/B) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0=set OPA/B~ to high: Disable interrupt output
1=set OPA/B~ to low: Enable interrupt output

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (SINA/B, CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ and OPA/B~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST16C2450 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C2450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to ST16C450-OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to ST16C450-OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
ST16C2450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C2450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals

SIGNALS	RESET STATE
TXA/B	High
OPA/B~	High
RTSA/B~	High
DTRA/B~	High

3

ST16C2450 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	INT enable	OP1~	RTS~	DTR~
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

3

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

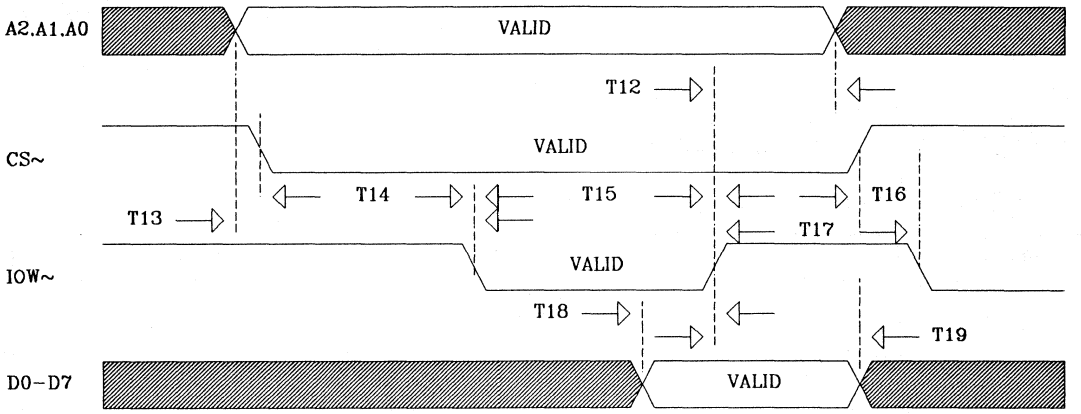
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

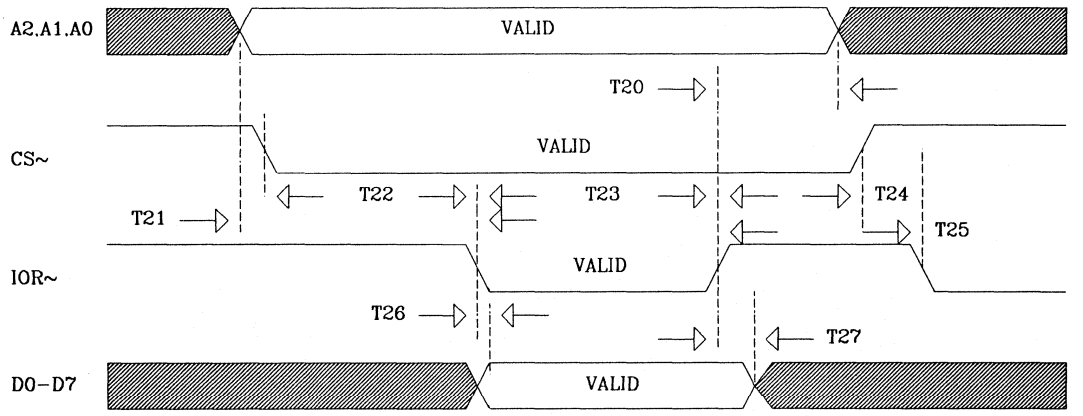
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

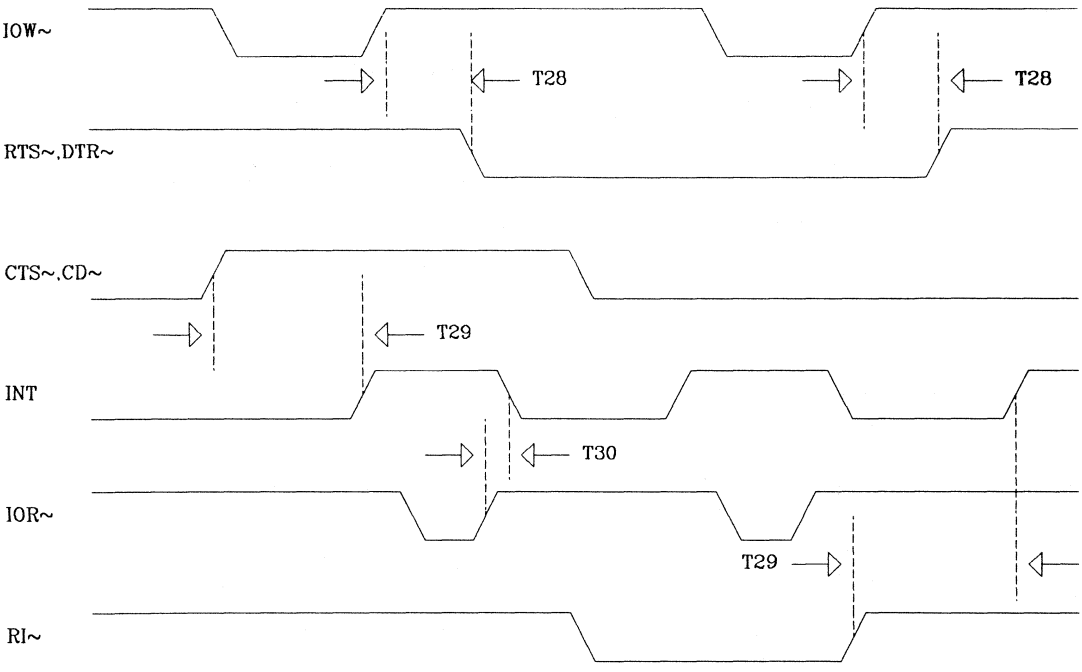


READ CYCLE TIMING



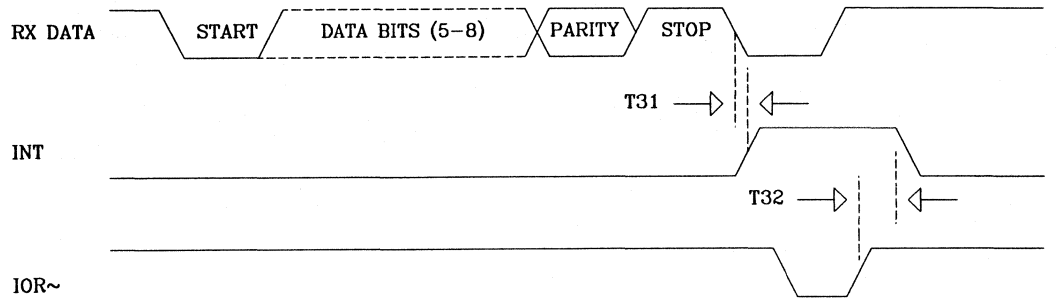
TIMING DIAGRAM

MODEM TIMING

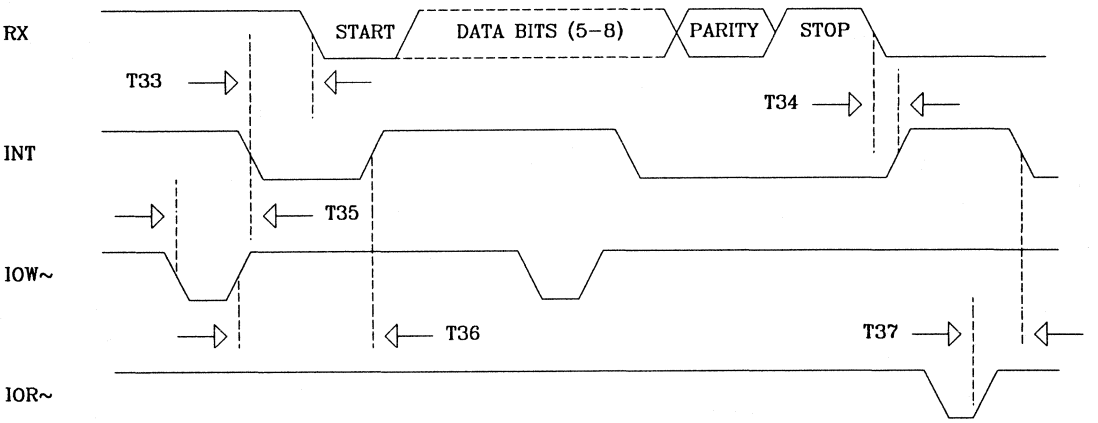


TIMING DIAGRAM

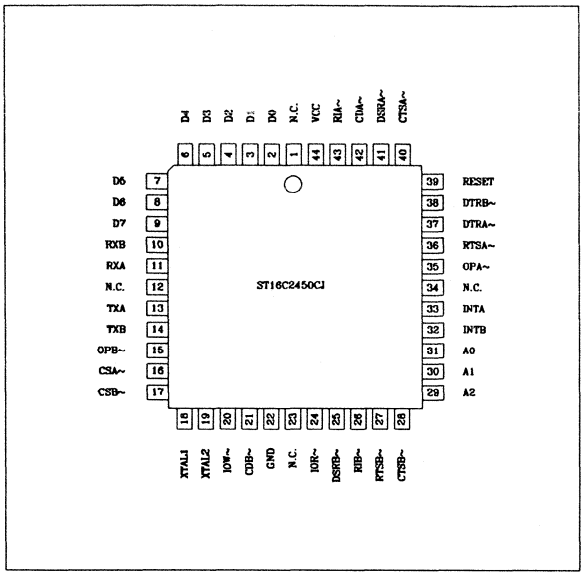
RECEIVER TIMING



TRANSMITTER TIMING



44 Pin PLCC pinout



STARTECH

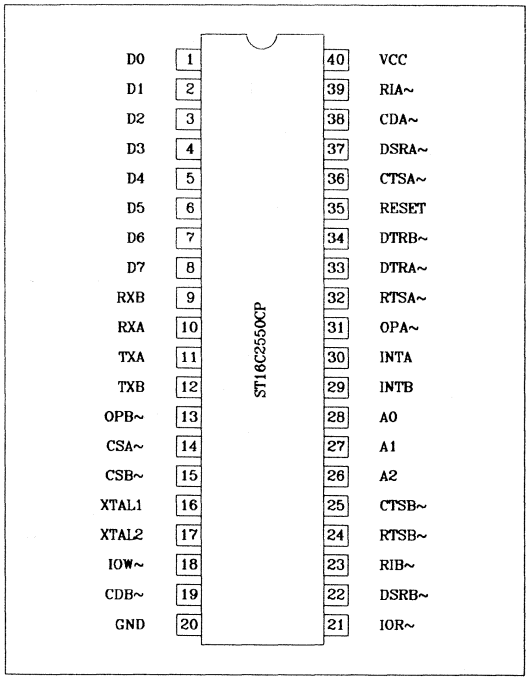
ST16C2550

MAY 1991

DUAL ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

DESCRIPTION

The ST16C2550 is a dual universal asynchronous receiver and transmitter with FIFO and modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C2550 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Dual ST16C550
* 16 byte transmit
* 16 byte receive FIFO with error flags
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

APPLICATIONS

* Dual serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* Fax
* Terminals

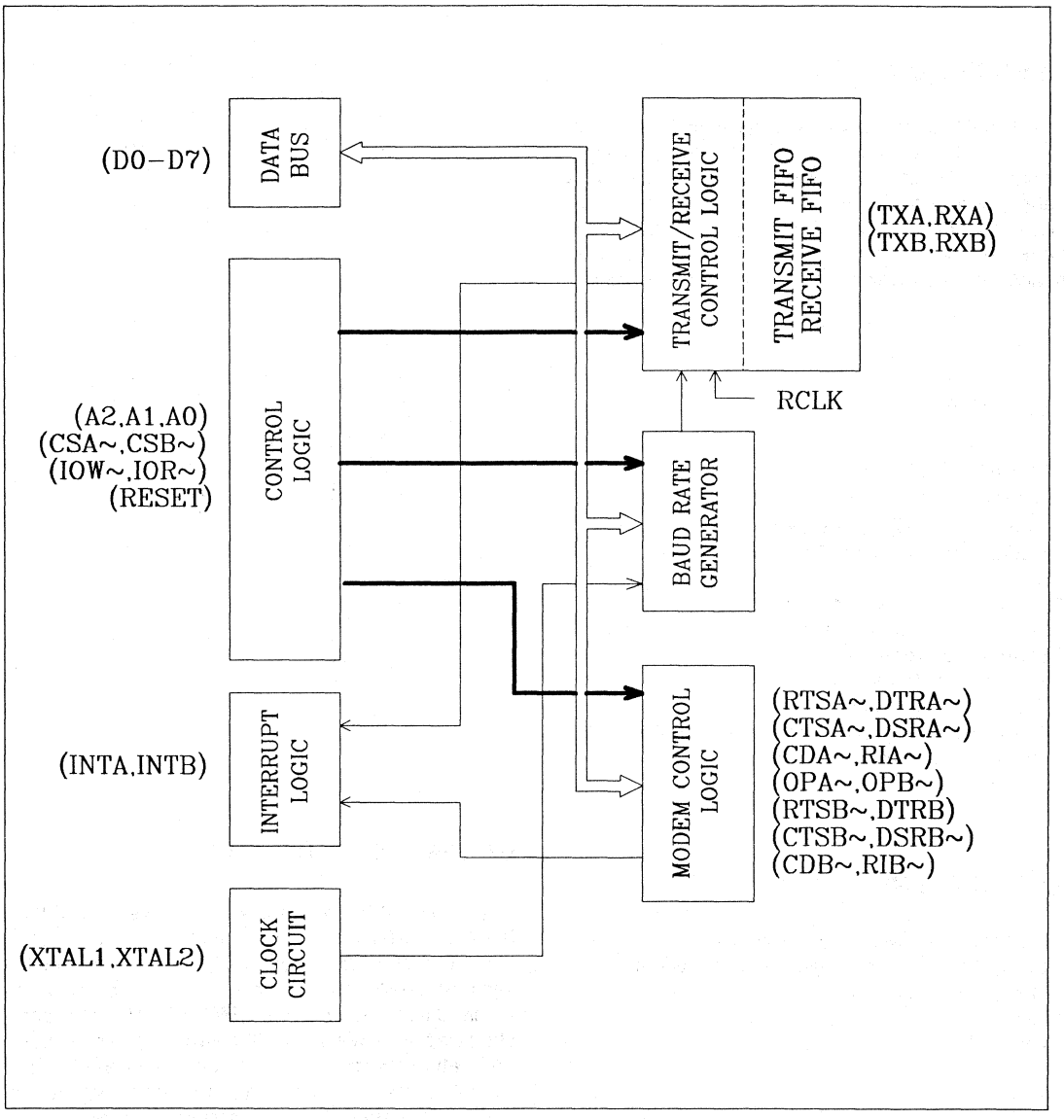
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2550CP40	Plastic	0° C to +70° C
ST16C2550CJ44	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C2550 is an improved, dual version of the NS16550 UART with higher speed operating access time. The ST16C2550 performs the parallel to serial/ serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C2550 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	description
D0-D7	1-8	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RXB	9	I	Serial data input B. The serial information received from MODEM or RS232 to ST16C2550 receive B circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally.
RXA	10	I	Serial data input A . The serial information received from MODEM or RS232 to ST16C2550 receive A circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXA input is disabled from external connection and connected to the TXA output internally.
TXA	11	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TXA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
TXB	12	O	Serial data output B. The serial data of channel B is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
OPB~	13	O	General purpose output. (active low) User defined output. See bit-3 modem control register B.
CSA~	14	I	Chip select A. (active low) A low at this pin will enable the UARTA/ CPU data transfer operation.
CSB~	15	I	Chip select B. (active low) A low at this pin will enable the UARTB/ CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2. See XTAL1.
IOW~	18	I	I/O write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
CDB~	19	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the modem B.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
GND	20	O	Signal and power ground.
IOR~	21	I	I/O read strobe. (active low) A low level on this pin will transfer the contents of the ST16C2550 data bus to the CPU.
DSRB~	22	I	Data set ready B. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART B.
RIB~	23	I	Ring detect B indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTSB~	24	O	Request to send B. (active low) To indicate that transmitter B has data ready to send. Writing a "1" in the modem control register B (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	25	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
A2	26	I	Address line 2. To select internal registers.
A1	27	I	Address line 1. To select internal registers.
A0	28	I	Address line 0. To select internal registers.
INTB	29	O	Interrupt output B. (active high) This pin goes high (when enabled by the interrupt enable register B) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART B.
INTA	30	O	Interrupt output A. (active high) This pin goes high (when enabled by the interrupt enable register A) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A.
OPA~	31	O	General purpose output A. (active low) User defined output. See bit-3 modem control register A.
RTSA~	32	O	Request to send A. (active low) To indicate that transmitter A has data ready to send. Writing a "1" in the modem control register A (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTRA~	33	O	Data terminal ready A. (active low) To indicate that ST16C2550 (channel A) is ready to receive data. This pin can be controlled via the modem control register A (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
DTRB~	34	O	Data terminal ready B. (active low) To indicate that ST16C2550 (channel B) is ready to receive data. This pin can be controlled via modem control register B (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTSA~	36	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
DSRA~	37	I	Data set ready A. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART A.
CDA~	38	I	Carrier detect A. (active low) A low on this pin indicates that carrier has been detected by the modem A.
RIA~	39	I	Ring detect A indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
Vcc	40	I	Power supply input.
TXRDYA~	1*	O	Transmit ready A (active low). This pin goes low when the transmit FIFO of the ST16C2550 A section is full. It can be used as a single or multi-transfer DMA.
TXRDYB~	12*	O	Transmit ready B (active low). This pin goes low when the transmit FIFO of the ST16C2550 B section is full. It can be used as a single or multi-transfer DMA.
RXRDYA~	23*	O	Receive ready A (active low). This pin goes low when the receive FIFO of the ST16C2550 A section is full. It can be used as a single or multi-transfer DMA.
RXRDYB~	34*	O	Receive ready B (active low). This pin goes low when the receive FIFO of the ST16C2550 B section is full. It can be used as a single or multi-transfer DMA.

* PLCC package only

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	FIFO Control Register A
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	FIFO Control Register B
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
B) LSR BIT4-1 will specify which error(s) has occurred.
C) LSR BIT-5 will indicate when the transmit FIFO is empty.
D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST16C2550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A/B
The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The ST16C2550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C2550 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	0	0	0	LSR A/B (Receiver Line Status Register)
2	0	0	0	RXRDY A/B (Received Data Ready)
3	0	0	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in ST16C450 mode and **BIT 6-7**: are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0 = No change.
1 = Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0 = No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0 = No change.
1 = Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5 = 1 and LCR BIT-4 = 1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TXA/B) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0=set OPA/B~ to high: Disable interrupt outputs
1=set OPA/B~ to low: Enable interrupt outputs

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ and OPA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST16C2550 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C2550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to ST16C550-OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to ST16C550-OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
ST16C2550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C2550 EXTERNAL RESET CONDITION

REGIISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BIT7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals

SIGNALS	RESET STATE
TXA/B	High
OPA/B~	High
RTSA/B~	High
DTRA/B~	High

ST16C2550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	OP1~	RTS~	DTR~
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

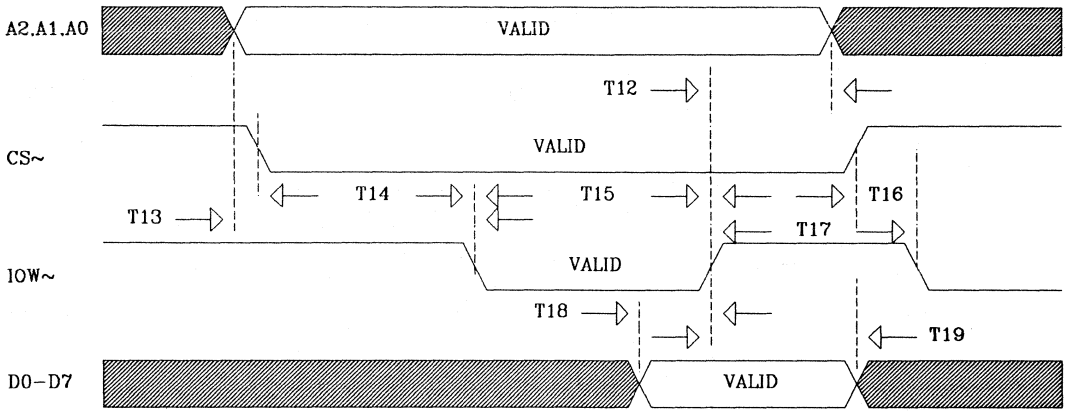
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

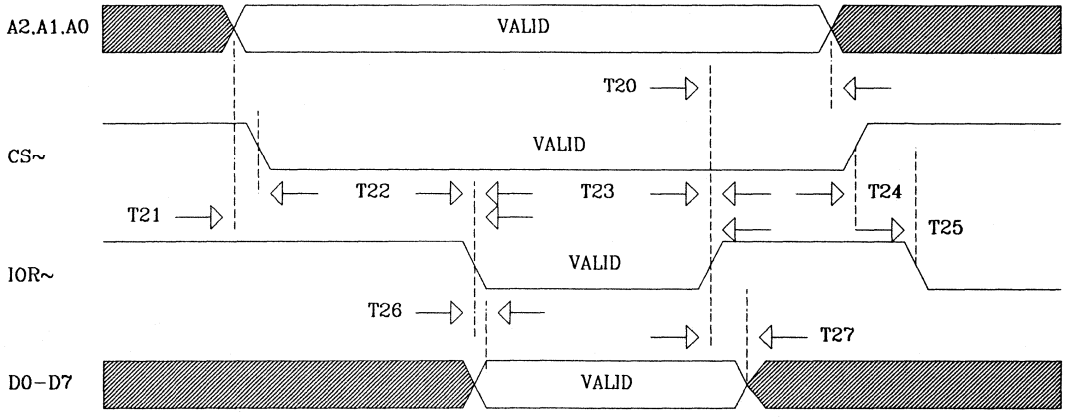
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

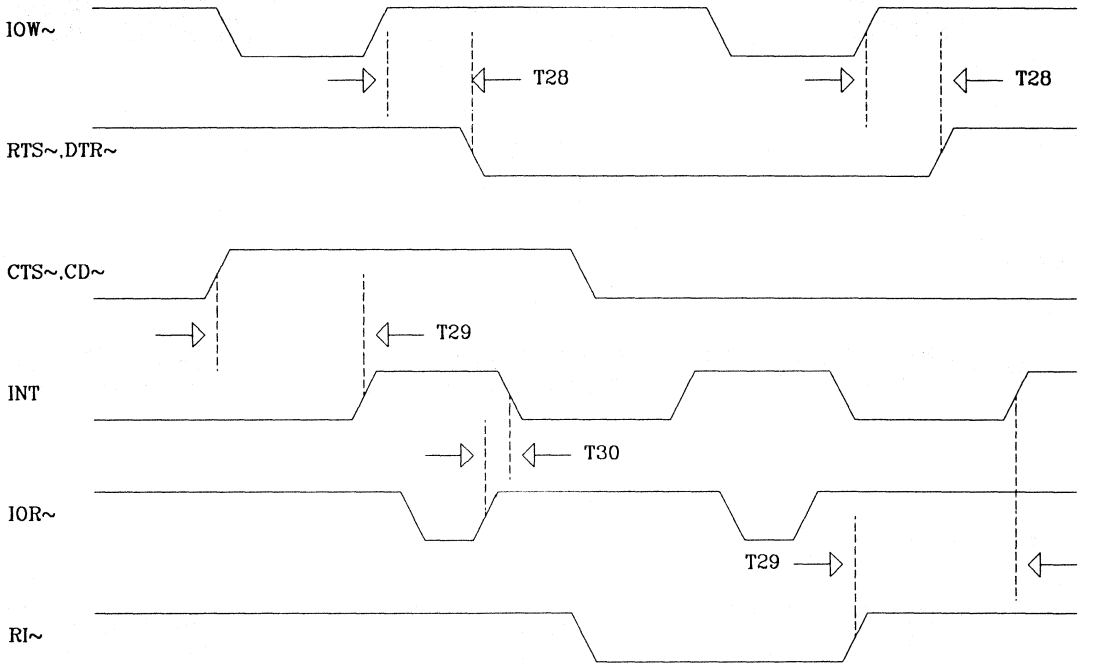


READ CYCLE TIMING



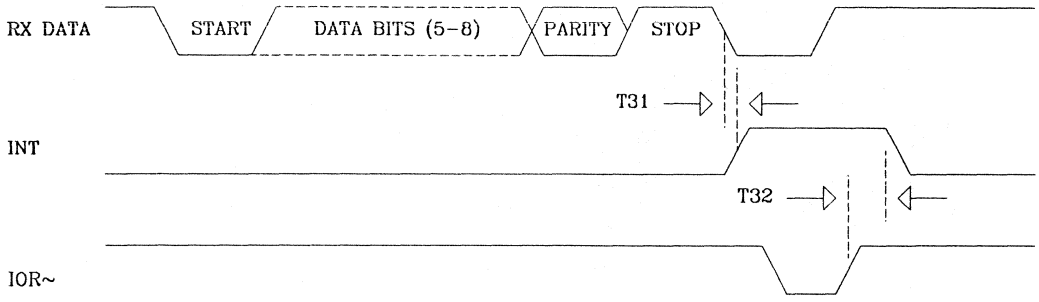
TIMING DIAGRAM

MODEM TIMING

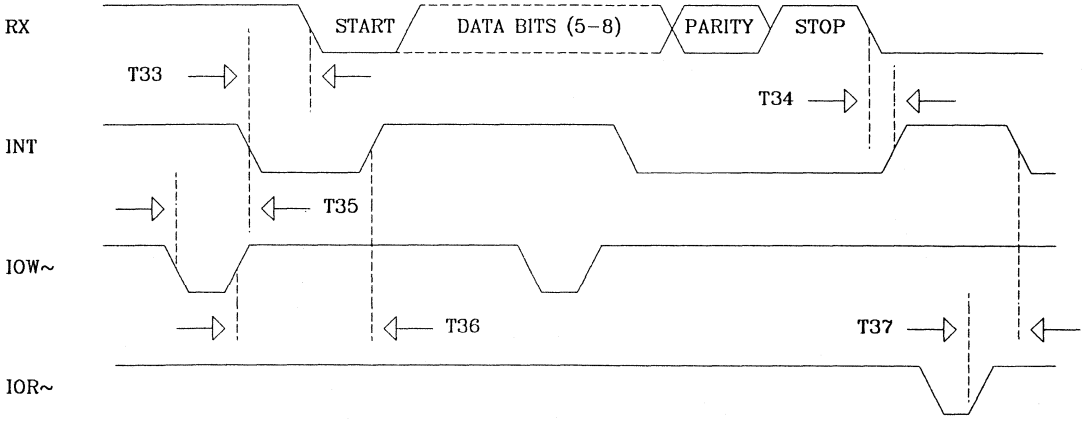


TIMING DIAGRAM

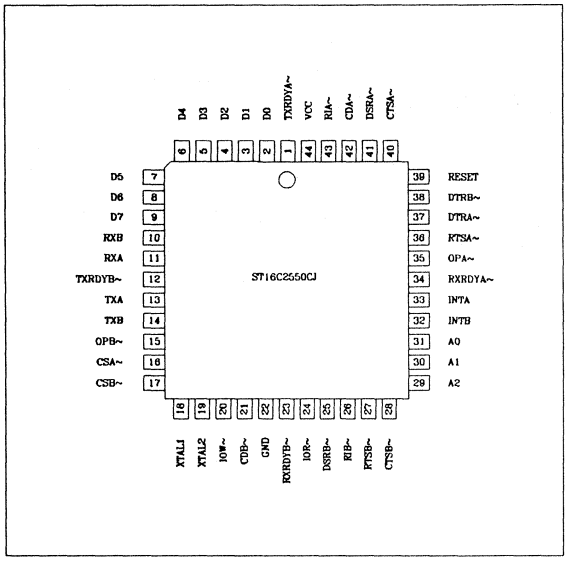
RECEIVER TIMING



TRANSMITTER TIMING



44 Pin PLCC pinout



STARTECH

ST68C554

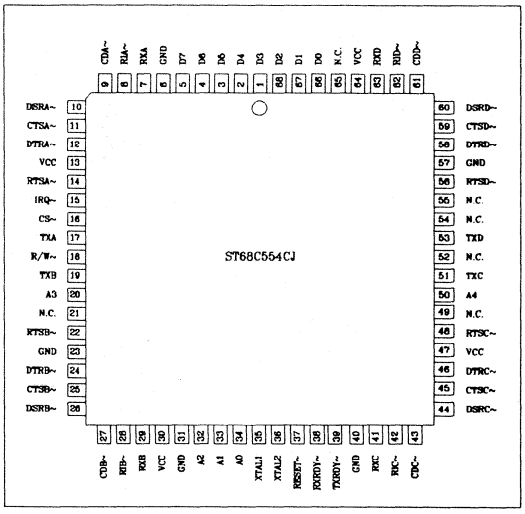
MAY 1991

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

3

DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST68C554 is fabricated in an advanced 1.2 u CMOS process to achieve low drain power and high speed requirements.



FEATURES

* Motorola, Rockwell, Hitachi bus compatible
* Quad ST16C550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS~,RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz external clock source

APPLICATIONS

* Quad serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* Fax
* Terminals
* Main frame

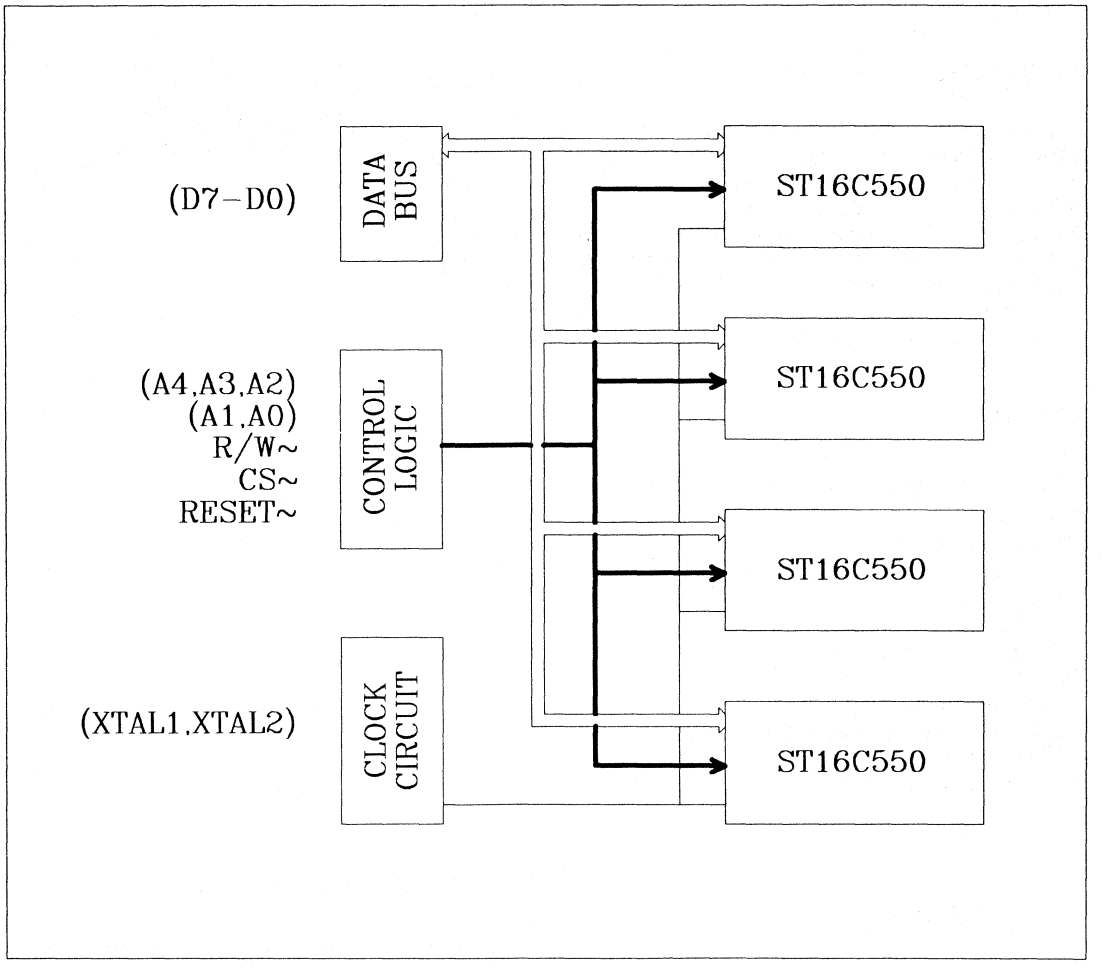
ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C554CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST68C554 is an improved, quad version of the NS16550 UART with higher speed operating access time. The ST68C554 performs the parallel to serial/ serial to parallel conversion on the data characters received from the CPU or the MODEM. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST68C554 can interface easily to the most popular microprocessors and communications link faults can

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	description
D7-D0	5-66	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS~	16	I	Chip select . (active low) A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
R/W~	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register.A high on this pin will transfer the contents of the ST68C554 data bus to the CPU.
CD A-B~ CD C-D~	9,27 43,61	I	Carrier detect A-D. (active low) A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.
DSR A-B~ DSR C-D~	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI A-B~ RI C-D~	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RTS A-B~ RTS C-D~	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A-B~ CTS C-D~	11,25 45,59	I	Clear to send A-D. (active low) The CTS~ signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ~	15	O	Interrupt output. (active low) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR A-B~ DTR C-D~	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST68C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET~	37	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.
TXRDY~	39	O	Transmit ready (active low). This pin goes low when the transmit FIFO of the ST68C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY~	38	O	Receive ready (active low). This pin goes low when the receive FIFO of the ST68C554 is full. It can be used as a single or multi-transfer DMA.

PROGRAMMING TABLE

CS~	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST68C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in

the receive FIFO.
B) LSR BIT4-1 will specify which error(s) has occurred.
C) LSR BIT-5 will indicate when the transmit FIFO is empty.
D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST68C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D
The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ~ output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable the receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST68C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C554 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	0	0	0	LSR A-D (Receiver Line Status Register)
2	0	0	0	RXRDY A-D (Received Data Ready)
3	0	0	0	TXRDY A-D (Transmitter holding register empty)
4	0	0	0	MSR A-D (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-5:
These bits are not used and are set zero.

ISR BIT 6-7:
0 = Normal mode.
1 = FIFO's are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit, when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit, when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0= Disable the IRQ~ outpout
1=Enable IRQ~ output.

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D~, DSR A-D~, CD A-D~, and RI A-D~) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D~, RTS A-D~ and OP A-D~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C554 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST68C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST68C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST68C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST68C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to ST16C550-OP1 in the MCR. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to ST16C550-OP2 in the MCR. It is the compliment to the CD~ input.

SCRATCHPAD REGISTER A-D
ST68C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86
112K	1	

ST68C554 EXTERNAL RESET CONDITION

REGIISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7=input signals

SIGNALS	RESET STATE
TX A-D	High
OP A-D~	High
RTS A-D~	High
DTR A-D~	High

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
200	2304	
300	1536	
600	768	
1200	384	
2400	192	
4800	96	
9600	48	
19.2K	24	
28.8K	16	
38.4K	12	
76.8K	6	
153.6K	3	
224K	2	2.86
448K	1	

ST68C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	IRQ enable	OP1~	RTS~	DTR~
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from Write	5			ns	
T_{13}	Write delay from address	25			ns	
T_{14}	Write delay from chip select	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from Write	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from Read	10			ns	
T_{22}	Read delay from chip select	10			ns	
T_{23}	Read strobe width	75			ns	
T_{24}	Chip select hold time from Read	0			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	

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AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial IRQ~ reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from Read to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from Read			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt		200	ns		100 pF load

* Baudout~ cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

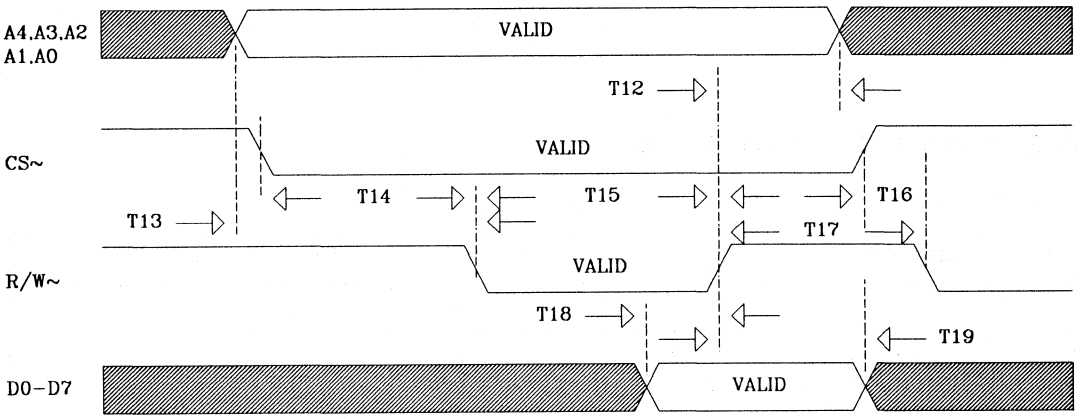
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

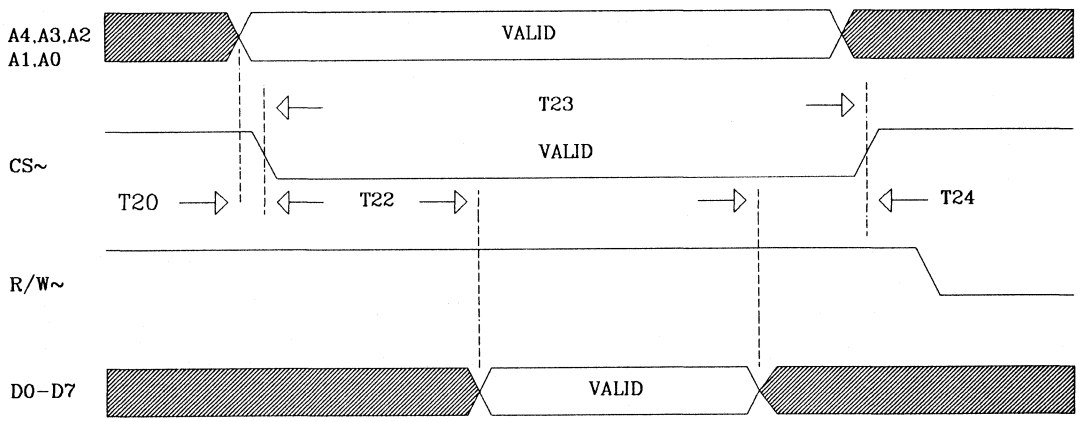
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

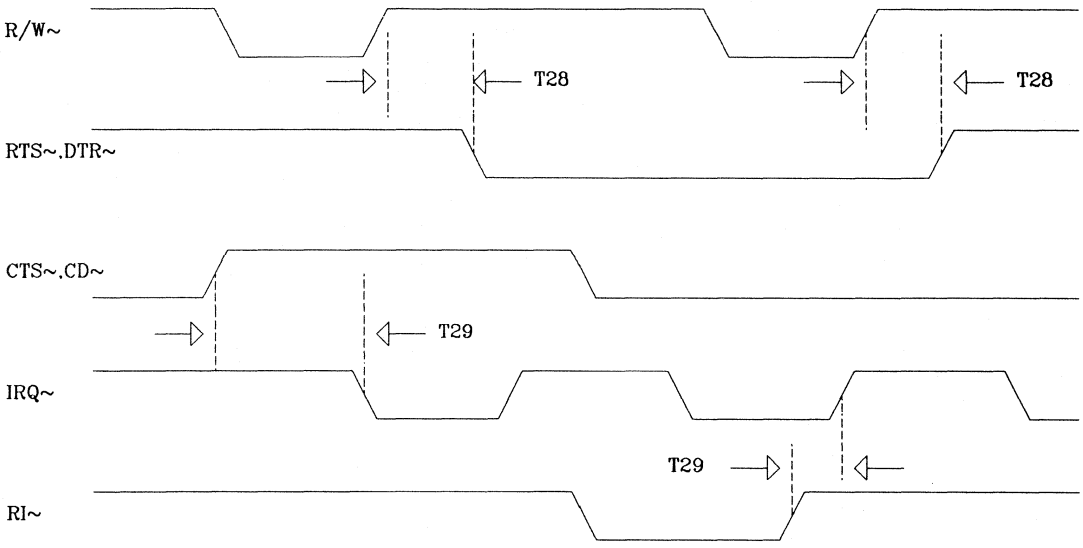


READ CYCLE TIMING



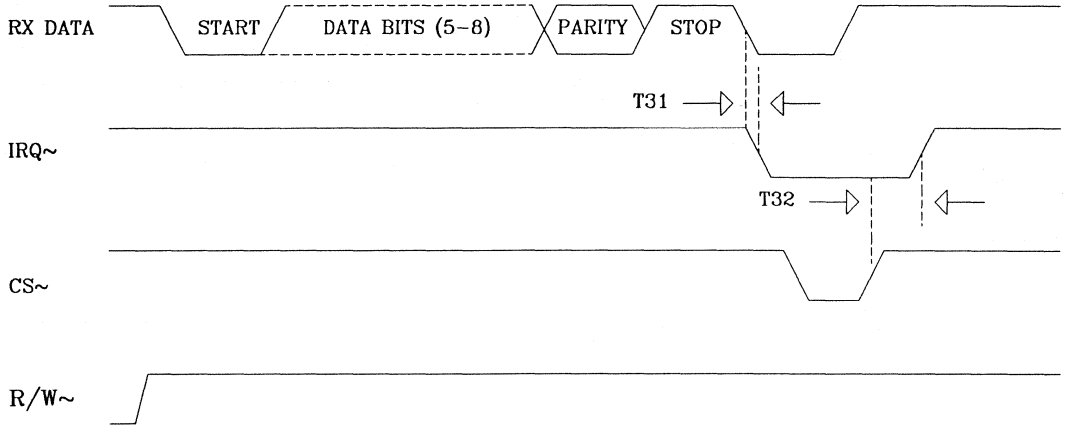
TIMING DIAGRAM

MODEM TIMING

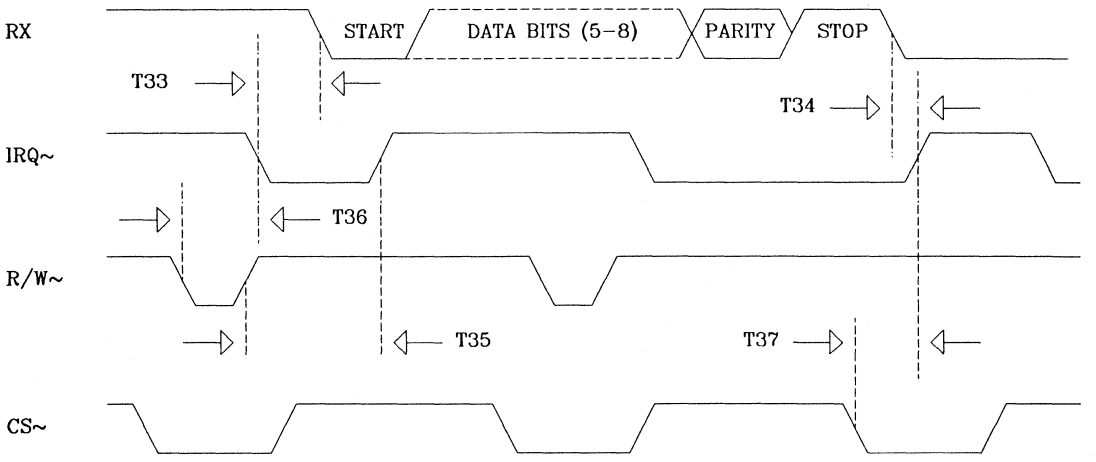


TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



UART/COMBO

4

STARTECH

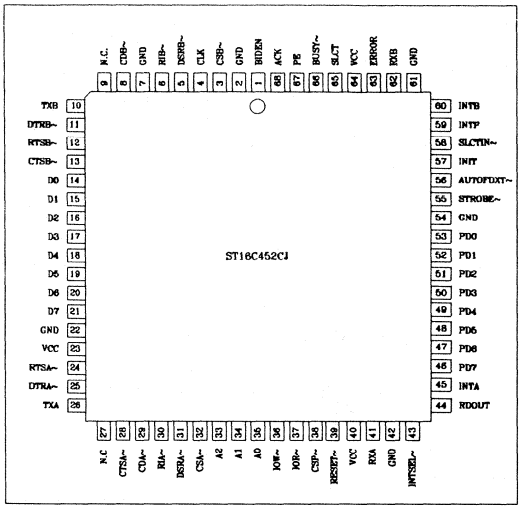
ST16C452

FEB 1991

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The ST16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C452 is fabricated in an advanced 1.2u CMOS process to achieve low power drain and high speed requirements.



FEATURES

* Pin-to-pin and functionally compatible to VL16C452
* Fully compatible with all new bidirectional PS/2 printer port registers
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Direct replacement of logic for PC/XT/AT
* High data transfer rate
* 448 kHz transmit/receive operation with 7.372 MHz external clock source

APPLICATIONS

* Dual serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* CENTRONICS printer port
* IBM PS/2 bidirectional printer port
* External bidirectional I/O
* IBM PC/XT/AT upgrade printer port

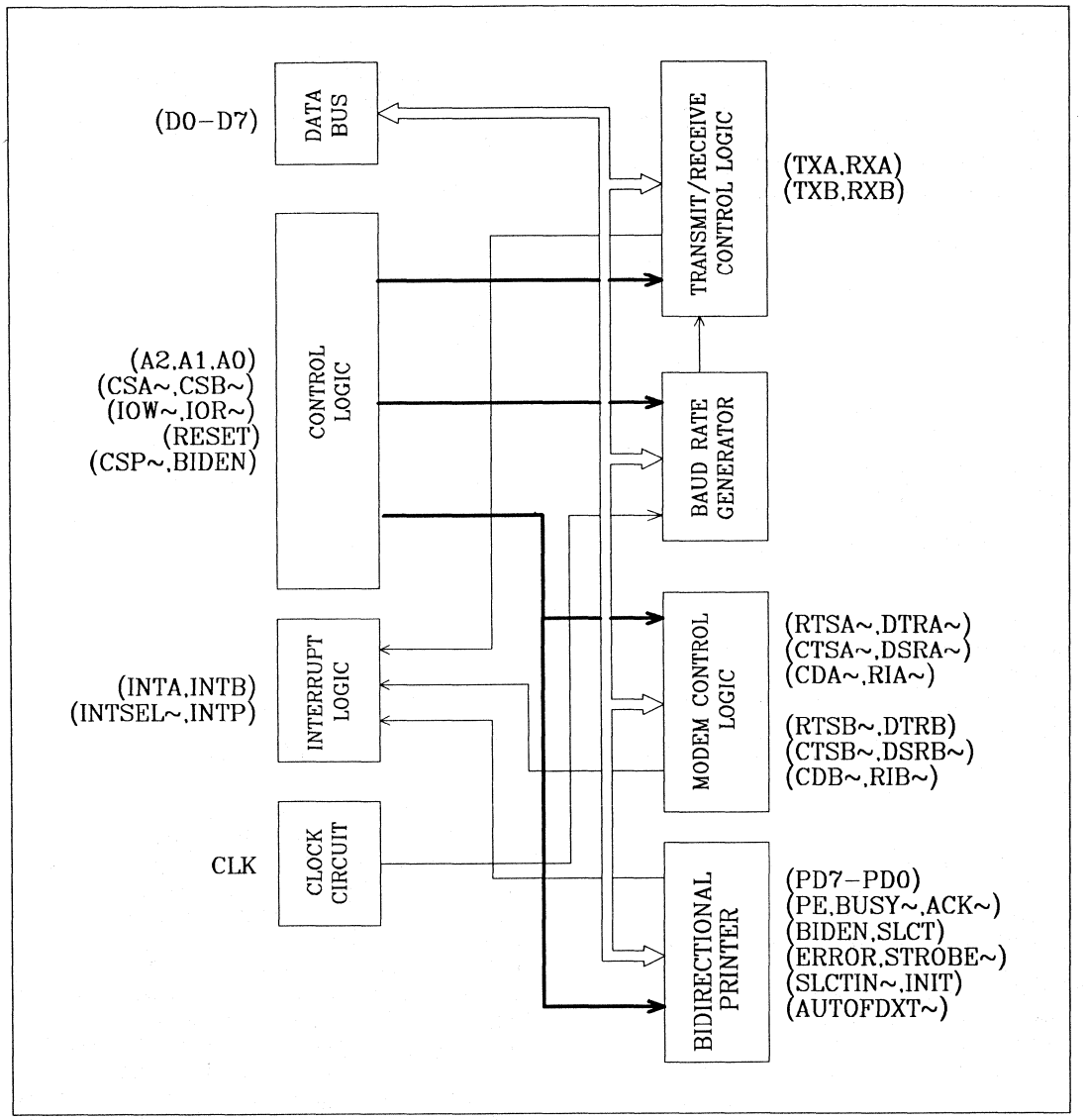
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C452CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C452 is an improved version of the VL16C452 with higher speed operating access time. The ST16C452 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The ST16C452 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. The ST16C452 also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C452 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
BIDEN	1	I	Printer direction select. A high puts the parallel port in the software controlled mode (input/output). A low puts the parallel port in the out mode.
CSB~	3	I	Chip select B. (active low) A low at this pin (while CSA~ and CSP~ = 1) will enable the UARTB / CPU data transfer operation.
CLK	4	I	External clock input. An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmission rates.
DSRB~	5	I	Data set ready B. (active low) A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
RIB~	6	I	Ring detect B indicator. (active low) A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
CDB~	8	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the MODEM B.
TXB	10	O	Serial data output B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTRB~	11	O	Data terminal ready B. (active low) To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RTSB~	12	O	Request to send B. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	13	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
D0-D7	14-21	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
RTSA~	24	O	Request to send A. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
DTRA~	25	O	Data trminal ready A. (active low) To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
TXA	26	O	Serial data output A. The serial data is transmitted via this pin with additional start , stop and parity bits. The TXA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CTSA~	28	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
CDA~	29	I	Carrier detect A. (active low) A low on this pin indicates that carrier has been detected by the MODEM A.
RIA~	30	I	Ring detect A indicator. (active low) A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
DSRA~	31	I	Data set ready A. (active low) A low on this pin indicates that MODEM A is ready to exchange data with UARTA.
CSA~	32	I	Chip select A. (active low) A low at this pin (while CSB~ and CSP~ = 1) will enable the UARTA / CPU data transfer operation.
A2	33	I	Address line 2. To select internal registers.
A1	34	I	Address line 1. To select internal registers.
A0	35	I	Address line 0. To select internal registers.
IOW~	36	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR~	37	I	Read strobe. (active low) A low level on this pin will transfer the contents of the ST16C452 data bus to the CPU.
CSP~	38	I	Chip select P. (active low) To enable the ST16C452 printer operation, this pin has to go low while CSA~ and CSB~ are high.
RESET~	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The parallel port of the ST16C452 will be set to output mode, the transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
RXA	41	I	Serial data input A. The serial information (data) received from MODEM or RS232 to ST16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode RXA input is disabled from external connection and connected to the TXA output internally.
INTSEL~	43	I	Interrupt select. (active low) The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to VCC, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
RDOUT	44	O	Read select out. A high on this pin indicates that the chip is being read by the CPU.
INTA	45	O	UART A interrupt output. (three state) This pin goes high (when enabled by MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
PD7-PD0	46-53	I/O	Bidirectional parallel ports. (three state) To transfer data in or out of the ST16C452 parallel port. PD7-PD0 are latched during output mode.
STROBE~	55	I/O	General purpose I/O or strobe output. (open drain active low) To transfer latched data to the external peripheral or printer.
AUTOFDXT~	56	I/O	General purpose I/O or line printer autofeed. (open drain active low) To signal the printer for continuous form feed.
INIT~	57	I/O	General purpose I/O or line printer initialize. (open drain active low) To signal the line printer to enter internal initialization routine.
SLCTIN~	58	I/O	General purpose I/O or line printer select. (open drain active low) To select the line printer.
INTP	59	O	Printer interrupt output. (high) To signal the state of the printer port.
INTB	60	O	UART B interrupt output. (three state) This pin goes high (when enabled by MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
RXB	62	I	Serial data input B. The serial information (data) received from MODEM or RS232 to ST16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
ERROR~	63	I	General purpose input or line printer error. (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected. (active high) This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy. (active high) An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty. (active high) An output from the printer to indicate out of paper.
ACK~	68	I	General purpose input or line printer acknowledge. (active low) An output from the printer to indicate that data has been accepted successfully.
GND	2,7,22 42,54, 61	O	Signal and power ground. All pins must be tied to ground.
VCC	23,40, 64	I	Power supply input. All pins must be tied to supply.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER A/B

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0=disable modem status register interrupt
1=enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C452 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level	Bit-2	Bit-1	Bit-0	Source of the interrupts
1	1	1	0	LSR A/B (Receiver Line Status Register)
2	1	0	0	RXRDY A/B (Received Data Ready)
3	0	1	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)
0	0	0	1	No interrupts

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5=1 and LCR BIT-4=1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TXA/B) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. ST16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four

bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
ST16C452 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customized Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the baud rate generator.

$$\text{divisor value (decimal)} = \frac{\text{input frequency}}{\text{baud rate x 16}}$$

$$\text{EXAMPLE: } \frac{1.8432 \times 10^6}{1200 \text{ (baud)} \times 16} = 96 \text{ (decimal)}$$

96 decimal = 0060 HEX
Divisor MSB = 00
Divisor LSR = 60

ST16C452 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
X	0	xxxxxxxx exp. AA Hex	OUTPUT
X	0	10101010	INPUT
0	1	xxxxxxxx	OUTPUT
1	1	xxxxxxxx	INPUT

REGISTER DESCRIPTIONS

PORT REGISTER
Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0 = BUSY input is in high state
1 = BUSY input is in low state

COMMAND REGISTER
The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0 = STROBE~ pin is in high state
1 = STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0 = AUTOFDXT~ pin is in high state
1 = AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0 = INIT pin is in low state
1 = INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0 = SLCTIN~ pin is in high state
1 = SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0 = Interrupt (INTP output) is disabled
1 = Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0 = STROBE~ output is set to high state
1 = STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0 = AUTOFDXT~ output is set to high state
1 = AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0 = INIT output is set to low state
1 = INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0 = SLCTIN~ output is set to high state
1 = SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0 = INTP output is disabled
1 = INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0 = PD7-PD0 are set for output mode
1 = PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER
Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or any other value for output.

ST16C452 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
TXA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high
AUTOFDXT~	Output mode, high
INIT	Output mode, low
SLCTIN~	Output mode, high

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1 = No interrupt 0 = Interrupt (PS/2 only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0 = IRQ disabled 1 = IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
--	--	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	0 = Output (PS/2 only) 1 = Input (PS/2 only) X = AT only		0 = INTP output disabled 1 = INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

* Baud rate cycle

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load
PRINTER PORT						
T_{38}	Delay from rising IOW~ to output data.	5			ns	
T_{39}	ACK~ pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK~ low to interrupt high.	5			ns	
T_{43}	Delay from IOR~ to reset interrupt.	5			ns	

ABSOLUTE MAXIMUM RATINGS

Operating Supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

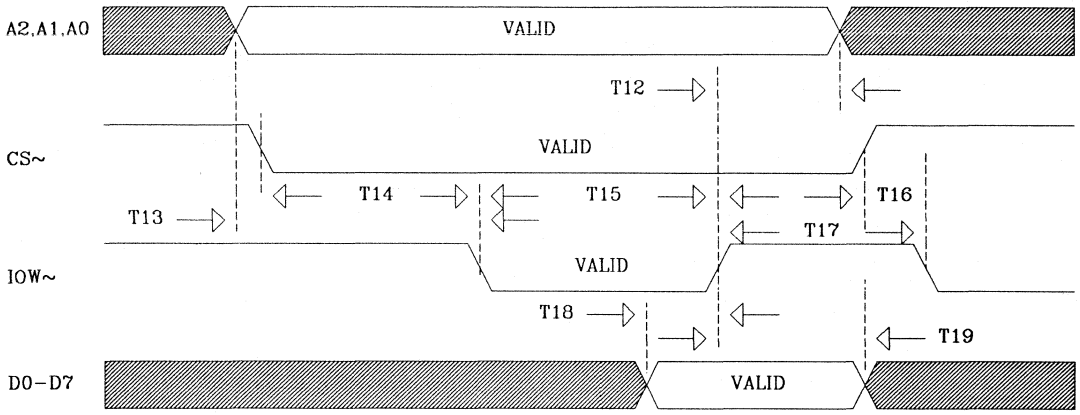
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

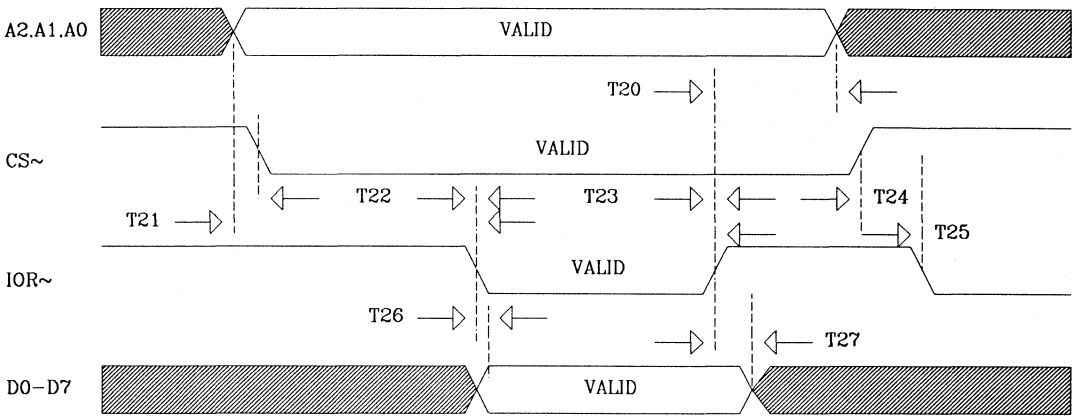
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

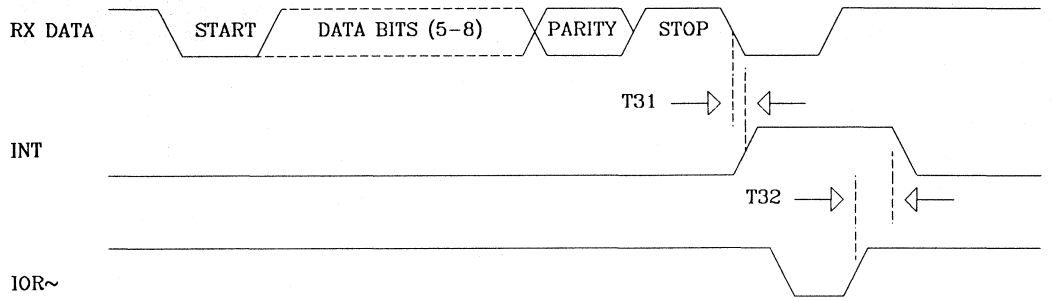


READ CYCLE TIMING

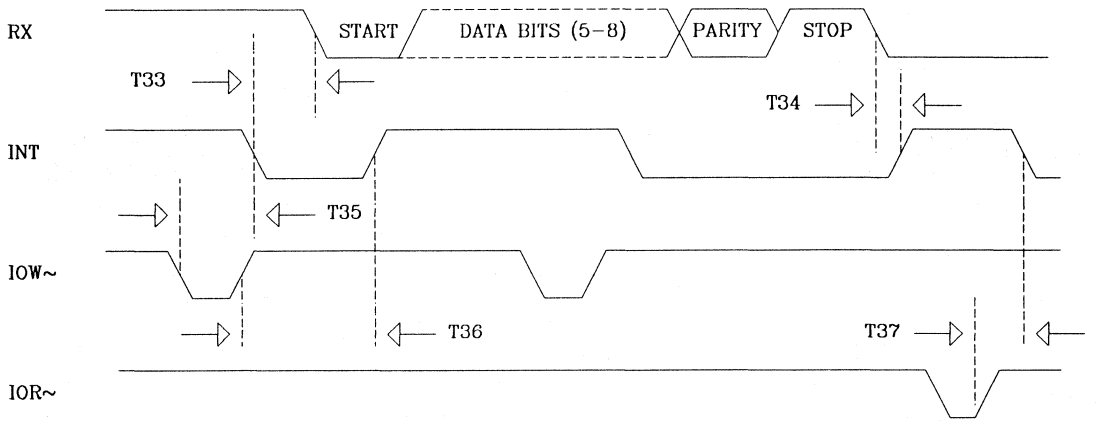


TIMING DIAGRAM

RECEIVER TIMING

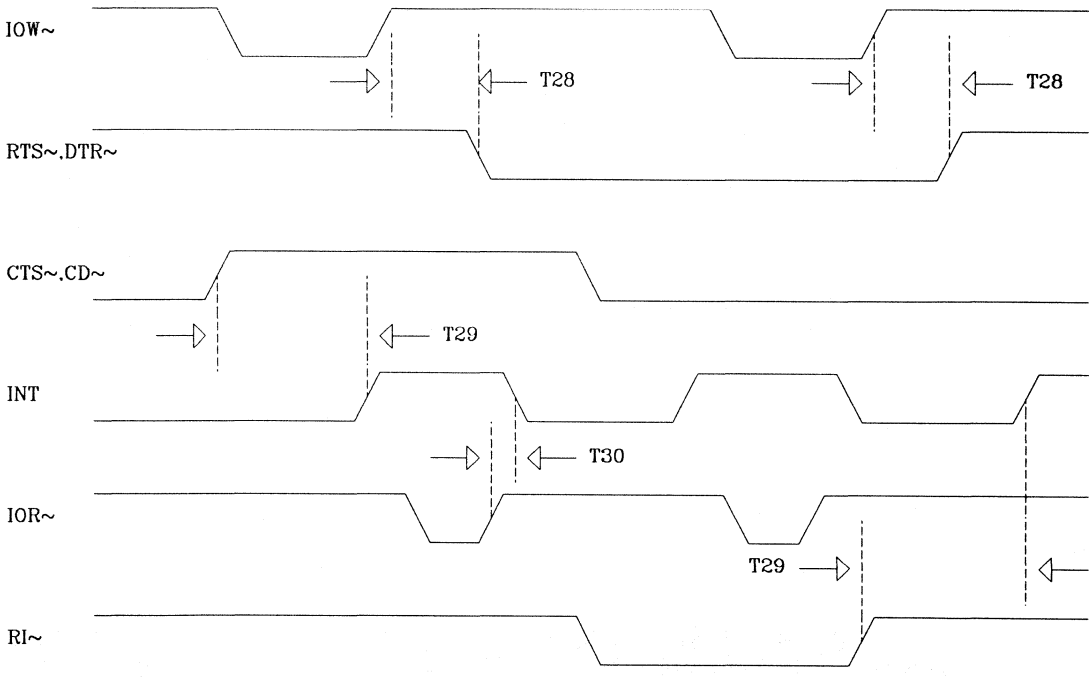


TRANSMITTER TIMING



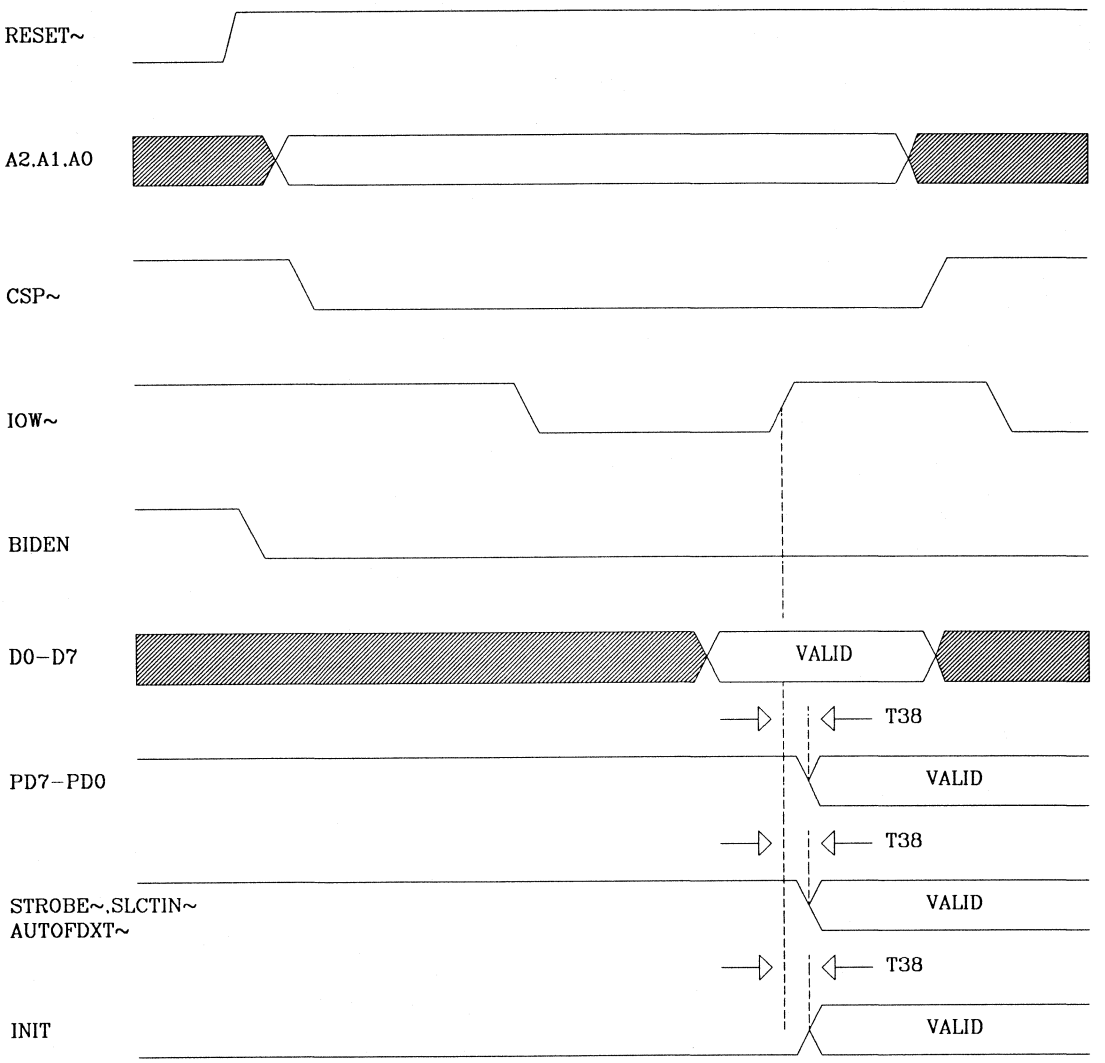
TIMING DIAGRAM

MODEM TIMING



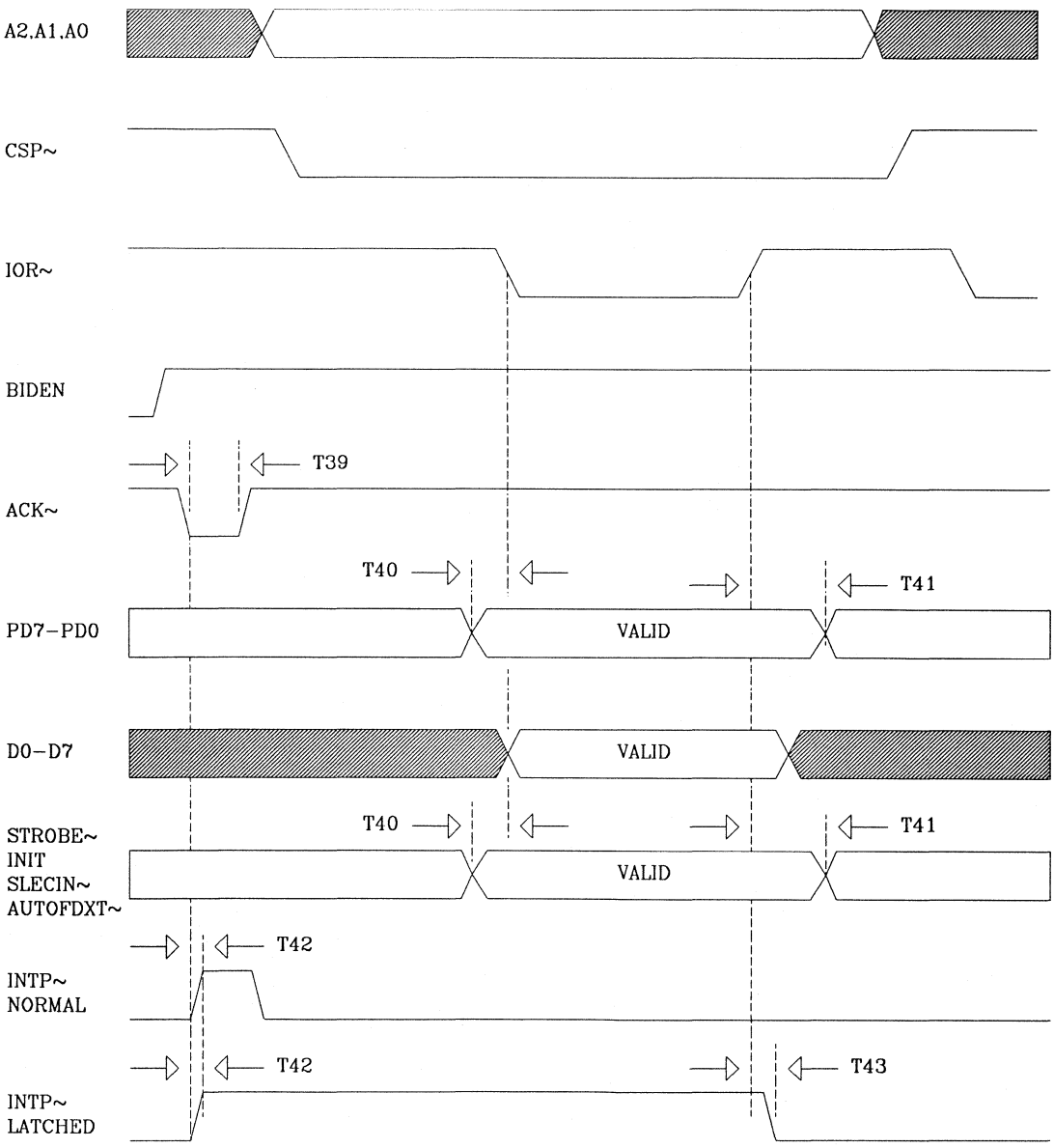
TIMING DIAGRAM

PRINTER WRITE OPERATION



TIMING DIAGRAM

PRINTER READ OPERATION



STARTECH

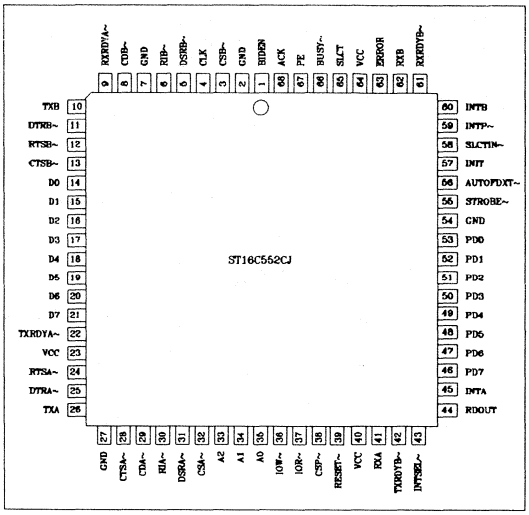
ST16C552

MAY 1991

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

DESCRIPTION

The ST16C552 is a dual universal asynchronous receiver and transmitter with FIFO and a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C552 is fabricated in an advanced 1.2u CMOS process to achieve low power drain and high speed requirements.



FEATURES

* Pin-to-pin and functionally compatible to VL16C552
* Fully compatible with all new bidirectional PS/2 printer port
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Direct replacement of logic for PC/XT/AT
* 448 kHz transmit/receive operation with 7.372 MHz external clock source

APPLICATIONS

* Dual serial receiver and/or transmitter
* Serial to parallel / parallel to serial converter
* Modem handshaking
* CENTRONICS printer port
* IBM PS/2 bidirectional printer port
* External bidirectional I/O
* IBM PC/XT/AT upgrade printer port

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C552CJ68	PLCC	0° C to +70° C

GENERAL DESCRIPTION

The ST16C552 is an improved version of the VL16C552 with higher speed operating access time. The ST16C552 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The ST16C552 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. The ST16C552 also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The ST16C552 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

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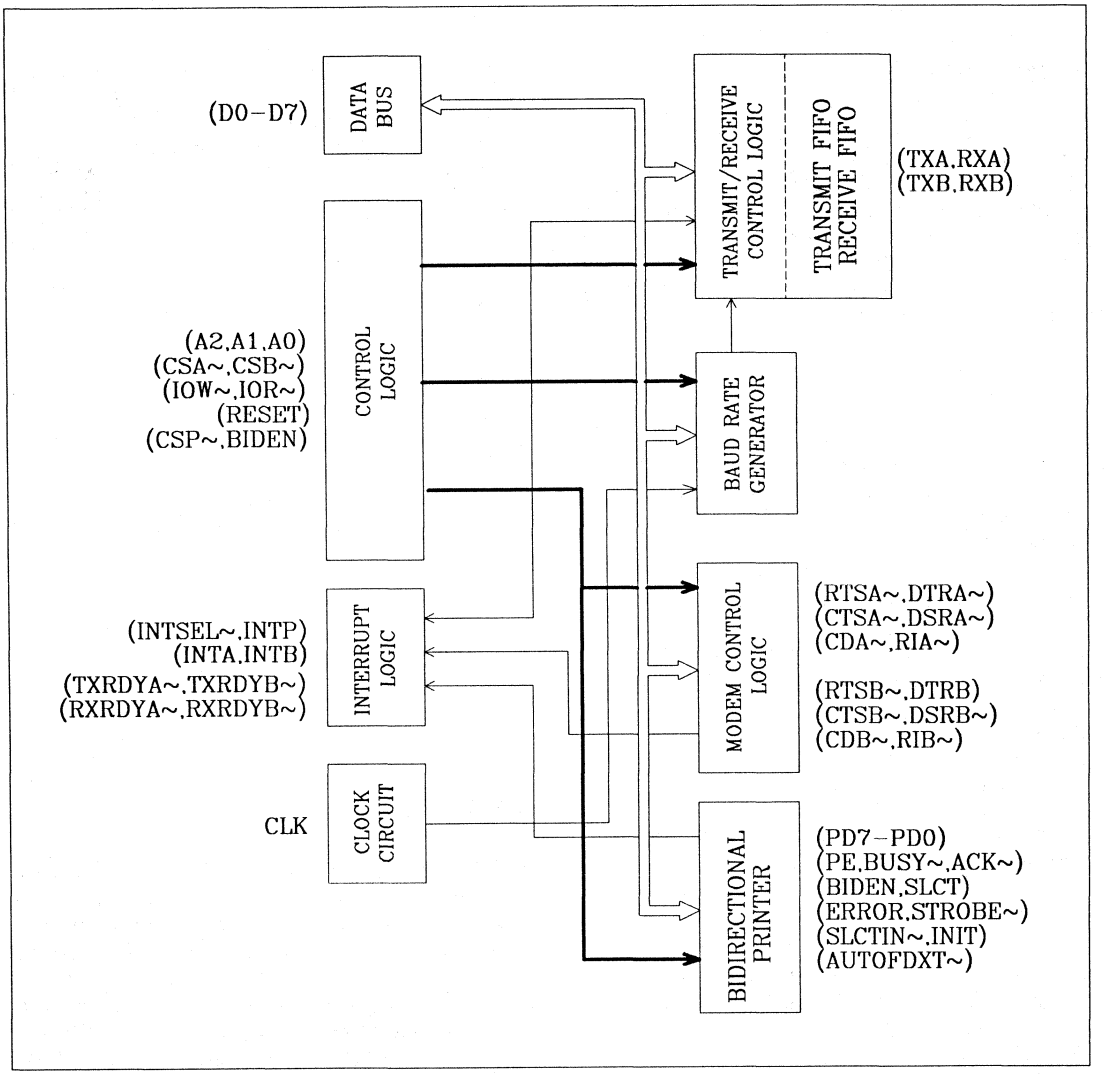
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
BIDEN	1	I	Printer direction select. A high puts the parallel port in the software controlled mode (input/output). A low puts the parallel port in the out mode.
CSB~	3	I	Chip select B. (active low) A low at this pin (while CSA~ and CSP~ = 1) will enable the UARTB / CPU data transfer operation.
CLK	4	I	External clock input. An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmission rates.
DSRB~	5	I	Data set ready B. (active low) A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
RIB~	6	I	Ring detect B indicator. (active low) A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
CDB~	8	I	Carrier detect B. (active low) A low on this pin indicates that carrier has been detected by the MODEM B.
RXRDYA~	9	O	Receive ready A (active low). This pin goes low when the receive FIFO of the ST16C552 A section is full. It can be used as a single or multi-transfer DMA .
TXB	10	O	Serial data output B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTRB~	11	O	Data terminal ready B. (active low) To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
RTSB~	12	O	Request to send B. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTSB~	13	I	Clear to send B. (active low) The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
D0-D7	14-21	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
TXRDYA~	22	O	Transmit ready A (active low). This pin goes low when the transmit FIFO of the ST16C552 A section is full. It can be used as a single or multi-transfer DMA.
RTSA~	24	O	Request to send A. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.
DTRA~	25	O	Data terminal ready A. (active low) To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
TXA	26	O	Serial data output A. The serial data is transmitted via this pin with additional start , stop and parity bits. The TXA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CTSA~	28	I	Clear to send A. (active low) The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
CDA~	29	I	Carrie detect A. (active low) A low on this pin indicates that carrier has been detected by the MODEM A.
RIA~	30	I	Ring detect A indicator. (active low) A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
DSRA~	31	I	Data set ready A. (active low) A low on this pin indicates that MODEM A is ready to exchange data with UARTA.
CSA~	32	I	Chip select A. (active low) A low at this pin (while CSB~ and CSP~ = 1) will enable the UARTA / CPU data transfer operation.
A2	33	I	Address line 2. To select internal registers.
A1	34	I	Address line 1. To select internal registers.
A0	35	I	Address line 0. To select internal registers.
IOW~	36	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR~	37	I	Read strobe. (active low) A low level on this pin will transfer the contents of the ST16C552 data bus to the CPU.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
CSP~	38	I	Chip select P. (active low) To enable the ST16C552 printer operation, this pin has to go low while CSA~ and CSB~ are high.
RESET~	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The parallel port of the ST16C552 will be set to output mode, the transmitter output and the receiver input will be disabled during reset time.
RXA	41	I	Serial data input A. The serial information (data) received from MODEM or RS232 to ST16C552 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode RXA input is disabled from external connection and connected to the TXA output internally.
TXRDYB~	42	O	Transmit ready B (active low). This pin goes low when the transmit FIFO of the ST16C552 B section is full. It can be used as a single or multi-transfer DMA.
INTSEL~	43	I	Interrupt select. (active low) The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to VCC, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
RDOUT	44	O	Read select out. A high on this pin indicates that the chip is being read by the CPU.
INTA	45	O	UART A interrupt output. (three state) This pin goes high (when enabled by MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
PD7-PD0	46-53	I/O	Bidirectional parallel ports. (three state) To transfer data in or out of the ST16C552 parallel port. PD7-PD0 are latched during output mode.
STROBE~	55	I/O	General purpose I/O or strobe output. (open drain active low) To transfer latched data to the external peripheral or printer.
AUTOFDXT~	56	I/O	General purpose I/O or line printer autofeed. (open drain active low) To signal the printer for continuous form feed.
INIT~	57	I/O	General purpose I/O or line printer initialize. (open drain active low) To signal the line printer to enter internal initialization routine.
SLCTIN~	58	I/O	General purpose I/O or line printer select. (open drain active low) To select the line printer.
INTP	59	O	Printer interrupt output. (high) To signal the state of the printer port.

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin description
INTB	60	O	UART B interrupt output. (three state) This pin goes high (when enabled by MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
RXRDYB~	61	O	Receive ready B (active low). This pin goes low when the receive FIFO of the ST16C552 B section is full. It can be used as a single or multi-transfer DMA .
RXB	62	I	Serial data input B. The serial information (data) received from MODEM or RS232 to ST16C552 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally.
ERROR~	63	I	General purpose input or line printer error. (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected. (active high) This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy. (active high) An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty. (active high) An output from the printer to indicate out of paper.
ACK~	68	I	General purpose input or line printer acknowledge. (active low) An output from the printer to indicate that data has been accepted successfully.
GND	2,7, 27,54	O	Signal and power ground. All pins must be tied to ground.
VCC	23,40, 64	I	Power supply input. All pins must be tied to supply.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	FIFO Control Register A
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	FIFO Control Register B
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A/B

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION
When FCR BIT-0 = 1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.
A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
B) LSR BIT4-1 will specify which error(s) has occurred.
C) LSR BIT-5 will indicate when the transmit FIFO is empty.
D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A/B
The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0 = disable receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable modem status register interrupt
1 = enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A/B
The ST16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the ST16C552 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1 = no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7**: are set "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0 = Disable the transmit and receive FIFO.
1 = Enable the transmit and receive FIFO.

FCR BIT-1:
0 = No change.
1 = Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0 = No change.
1 = Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0 = No change.
1 = Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A/B
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00 = 5 bits word length
01 = 6 bits word length
10 = 7 bits word length
11 = 8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0 = 1 stop bit , when word length = 5, 6, 7, 8 bits
1 = 1 and 1/2 stop bit , when word length = 5 bits
1 = 2 stop bits, word length = 6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0 = no parity
1 = a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0 = odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1 = an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = 1 and LCR BIT-4 = 0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5 = 1 and LCR BIT-4 = 1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1 = forces the transmitter output (TXA/B) to go low to alert the communication terminal
0 = normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0 = normal operation
1 = select divisor latch register

MODEM CONTROL REGISTER A/B
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0 = force DTR~ output to high
1 = force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A/B
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. ST16C552 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A/B
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the ST16C552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the ST16C552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the ST16C552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the ST16C552 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER A/B
ST16C552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0,
MSRA/B	BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
TXA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high

ST16C552 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
X	0	xxxxxxxx exp. AA Hex	OUTPUT
X	0	10101010	INPUT
0	1	xxxxxxxx	OUTPUT
1	1	xxxxxxxx	INPUT

REGISTER DESCRIPTIONS

PORT REGISTER
Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0 = an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1 = no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0 = ERROR~ input is in low state
1 = ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0 = SLCT input is in low state
1 = SLCT input is in high state

SR BIT-5:
PE input state.
0 = PE input is in low state
1 = PE input is in high state

SR BIT-6:
ACK~ input state.
0 = ACK~ input is in low state
1 = ACK~ input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER
The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0= STROBE~ pin is in high state
1= STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0= AUTOFDXT~ pin is in high state
1= AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state
1= SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state
1= STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state
1= AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0= SLCTIN~ output is set to high state
1= SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER
Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or any other value for output.

ST16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1 = No interrupt 0 = Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0 = IRQ disabled 1 = IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	0 = Output 1 = Input		0 = INTP output disabled 1 = INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time					
T_{12}	Address hold time from IOW~	5			ns	
T_{13}	IOW~ delay from address	25			ns	
T_{14}	IOW~ delay from chip select	10			ns	
T_{15}	IOW~ strobe width	50			ns	
T_{16}	Chip select hold time from IOW~	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{20}	Address hold time from IOR~	0			ns	
T_{21}	IOR~ delay from address	10			ns	
T_{22}	IOR~ delay from chip select	10			ns	
T_{23}	IOR~ strobe width	75			ns	
T_{24}	Chip select hold time from IOR~	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR~ to data			75	ns	100 pF load
T_{27}	IOR~ to floating data delay	0		50	ns	100 pF load

* Baud rate cycle

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
TRANSMITTER						
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW~ to reset interrupt					
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{37}	Delay from IOR~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{28}	Delay from IOW~ to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR~ to reset interrupt			200	ns	100 pF load
PRINTER PORT						
T_{38}	Delay from rising IOW~ to output data.	5			ns	
T_{39}	ACK~ pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK~ low to interrupt high.	5			ns	
T_{43}	Delay from IOR~ to reset interrupt.	5			ns	

ABSOLUTE MAXIMUM RATINGS

Operating Supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to V_{CC}+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

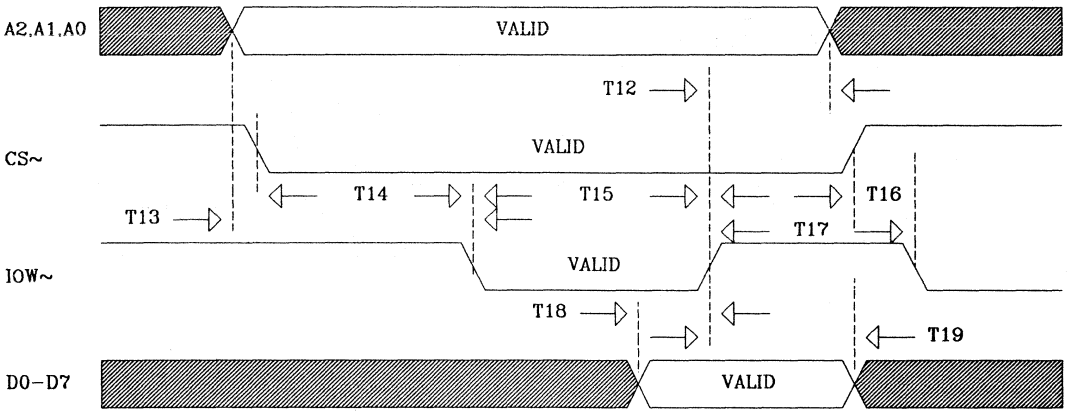
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

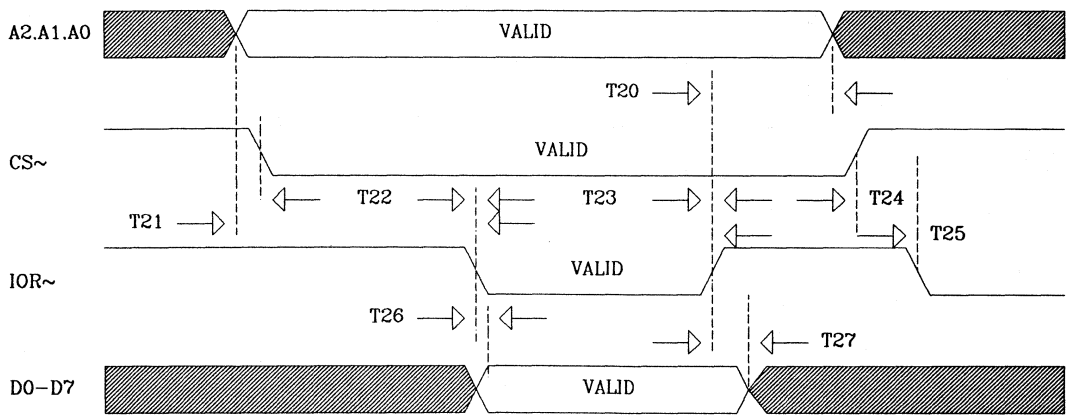
Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

TIMING DIAGRAM

WRITE CYCLE TIMING

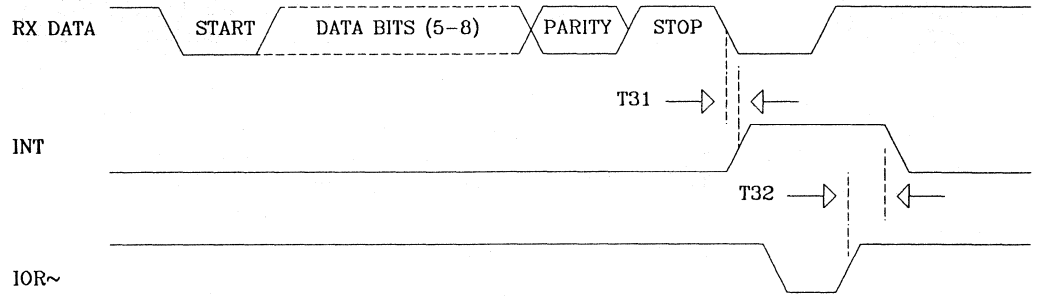


READ CYCLE TIMING

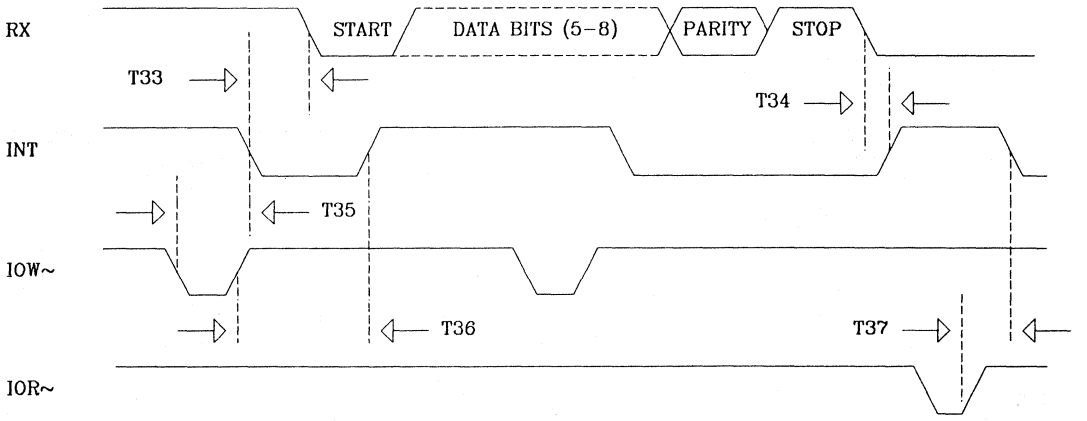


TIMING DIAGRAM

RECEIVER TIMING

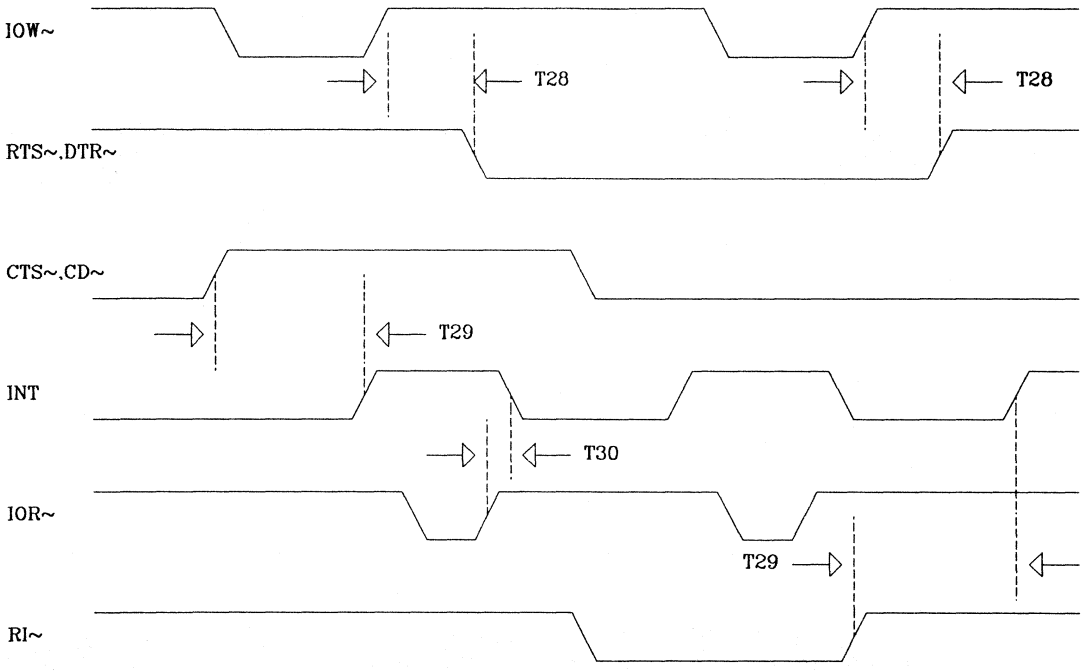


TRANSMITTER TIMING



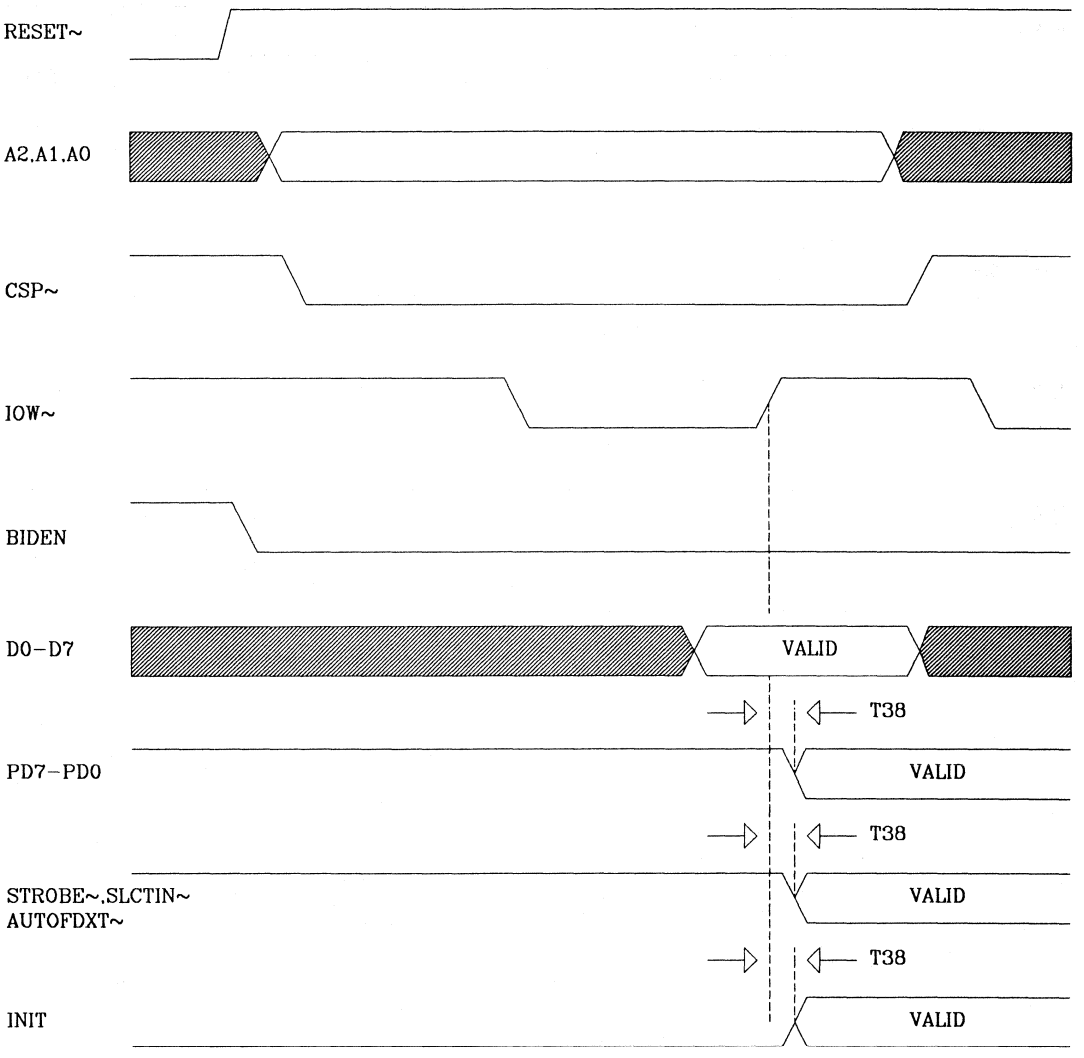
TIMING DIAGRAM

MODEM TIMING



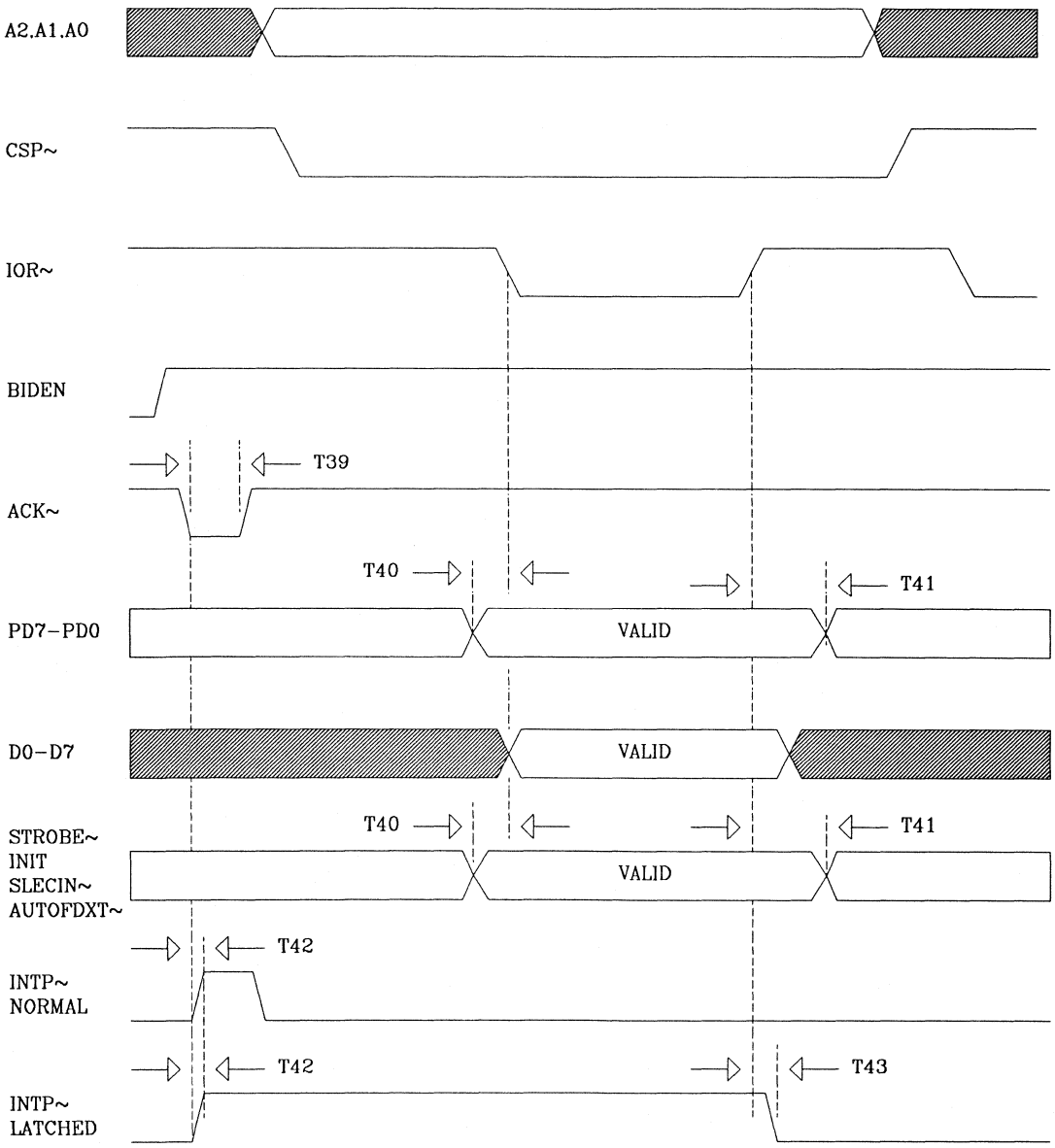
TIMING DIAGRAM

PRINTER WRITE OPERATION



TIMING DIAGRAM

PRINTER READ OPERATION



APPLICATION NOTES

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INTENTIONALLY LEFT BLANK FOR FUTURE EXPANSION

QUALITY/RELIABILITY

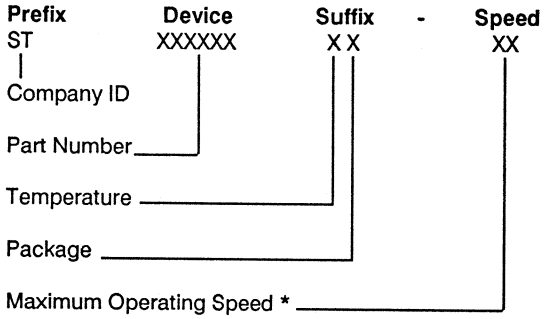
6

INTENTIONALLY LEFT BLANK FOR FUTURE EXPANSION

ORDERING INFORMATION

7

ORDERING INFORMATION AND PART NUMBERING GUIDE



Temperature Range

C	Commercial	0° C	To	+70° C
I	Industrial	-40° C	To	+85° C
M	Military	-55° C	To	+125° C

Package Type

P Plastic
C Ceramic
D Cerdip
L Leadless Chip Carrier (LCC)
J Plastic Leaded Chip Carrier (PLCC)
F Flat Pack
Q Quad Flat Pack
G Pin Grid

* General marking will not show this option unless, parts are tested for different operating speeds.

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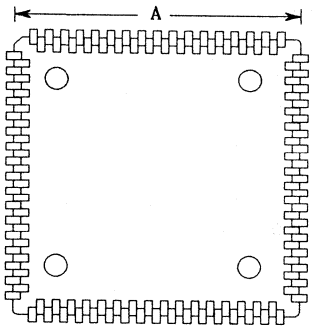
PACKAGING INFORMATION

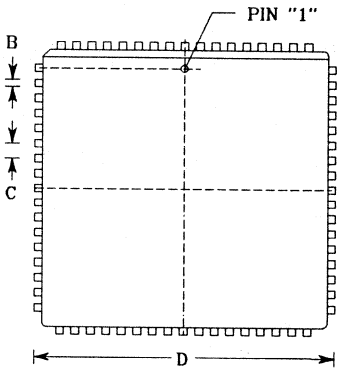
8

PLCC PACKAGING INFORMATION

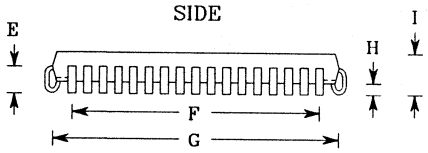
BACK



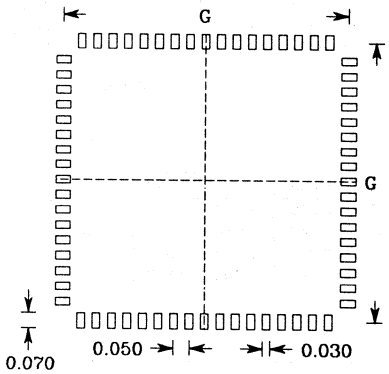
TOP



SIDE



	44PIN	52PIN	68PIN	84PIN
A	0.653	0.730	0.954	1.154
B	0.029	0.029	0.029	0.029
C	0.050	0.050	0.050	0.050
D	0.690	0.790	0.990	1.190
E	0.110	0.110	0.110	0.110
F	0.500	0.600	0.800	1.000
G	0.610	0.710	0.910	1.110
H	0.026	0.026	0.026	0.026
I	0.182	0.182	0.182	0.182



Recommended P.C.B. foot print

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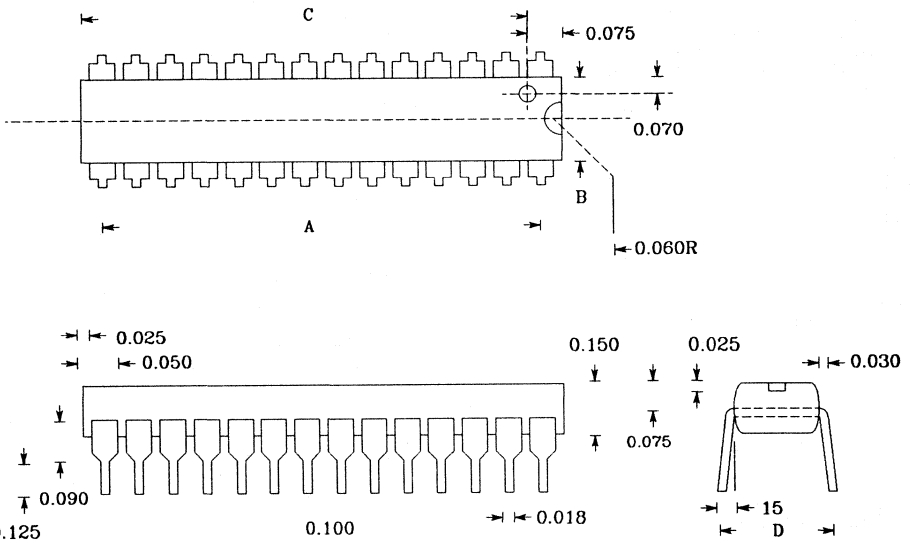
PLASTIC DIP PACKAGING INFORMATION



	16PIN	18PIN	28PIN	40PIN
A	0.700	0.800	1.300	1.900
B	0.248	0.248	0.512	0.512
C	0.748	0.945	1.445	2.028
D	0.300	0.300	0.600	0.600

REPRESENTATIVES

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North American Representatives

Alabama
NOVUS GROUP
TEL (205) 534-0044
FAX (205) 534-0186

California
H-TECHNICAL SALES
TEL (408) 453-2111
FAX (408) 453-3836

INFINITY SALES
TEL (714) 833-0300
FAX (714) 833-0303

INFINITY SALES
TEL (805) 966-9408

INFINITY SALES
TEL (213) 455-2566

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DYNAMIC SALES
TEL (203) 693-0451

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TEL (305) 970-9097
FAX (305) 975-9698

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FAX (404) 263-8946

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TEL (708) 285-1000
FAX (708)285-1008

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FAX (617) 273-4856

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FAX (616) 454-2680

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FAX (612) 854-9634

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FAX (919) 460-5703

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FAX (214) 934-0117

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FAX (512) 836-1695

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ELECTRONIC COMPONENT SALES
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FAX (206) 232-1095

ELECTRONIC COMPONENT SALES
TEL (509) 456-0100

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TEL (414) 786-1403
FAX (414) 786-1813

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Roseville, MN
TEL (800) 247-0867

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FAX (44) 3-72-376-848

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FAX (49) 6-031-61-788

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FAX (81) 3-326-43-419

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SERIAL SYSTEMS MKTG.
TEL (65) 293-8830
FAX (65) 291-2673